DC Offset Modeling and Noise Minimization for Differential Amplifier in Subthreshold Operation

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Abstract— **This work presents the rigorous formulation of input referred offset voltage for differential amplifier, having the input pair devices in subthreshold region of operation. The formulation has been verified in 0.35 µm and 0.18 µm CMOS technologies by using Monte Carlo Simulation. Minimization of 1/f noise is the additional advantage of this method.**

I. Introduction

The increasing demand of portable applications and battery operated systems gears up the interest in design methodology for low power consumption. For low power consumption, the devices operate either at low voltage or at low current or at both. Devices may pertain to weak, moderate or strong inversion region. Out of three regions, MOSFET operating in subthreshold region is most suitable for above requirement. The behavior of the MOSFET in subthreshold region has been investigated by many authors [1-4].

For low power and high precision analog integrated circuits, minimization of input offset voltage and noise is essential. Random device mismatches, which accrue during the fabrication process result in offset voltage. Study and impact analysis of random mismatches on the performance of analog integrated circuit have been carried out by many researchers [5-8].The work done by these authors provides only the cause and statistical parameters responsible for mismatches but do not provide the design procedure to reduce the offset voltage.

The popular methods available till date to minimize the offset and noise are trimming, chopper stabilization and auto zeroing [9-11]. Some amount of work has been done to minimize the offset voltage at device level, when device is in saturation [12], however, no such work has been found for subthreshold region.

In the present work, effort has been made to formulate the offset voltage, while the devices are operated in subthreshold region. The differential amplifier (diff-amp) is the input stage of two- or three-stage operational amplifiers. The input pair and current load devices of diff-amp are mainly responsible for offset and noise. We have developed mathematical formulation of input offset voltage for differential amplifier and verified it with simulation results.

A brief review of subthreshold region of operation for MOSFET is provided in section II. In section III, modeling of offset voltage for differential amplifier has been given and formulation of method has been provided. Noise minimization has been presented in section IV. Section V explains the design procedure to minimize the offset voltage in subthreshold region. In section VI, comparison between the calculated and simulated results has been given. Section VII, gives the conclusion.

II. Subthreshold Operation

For gate voltage less than threshold voltage, the applied gate potential not only affects the channel charge (as the case in saturation region) but also very small depletion charge. Thus, device conducts very small but finite current. As a result, the charge carriers in source region overcome the potential barrier to the substrate and enter the channel region exhibiting the similar phenomena of turning-on the bipolar transistor. This phenomenon leads the behavior of MOSFET similar to bipolar transistor [13, 14]. The well known equation for the MOS transistor operating in subthreshold region is given by [15]

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS}}{nV_T}\right) \quad (1)$$

Where, I_D is transistor bias current, I_{D0} is characteristic current, V_{GS} is gate to source voltage, $V_T = kT/q$ is thermal voltage and n is slope factor.

The transconductance of the device is,

$$g_m = \frac{I_D}{nV_T} \quad (2)$$

The above equation shows that, transconductance has a linear relationship with drain current and gets maximized in subthreshold region. However, the gain bandwidth and slew rate of the amplifier are always low as the devices are operated at very low drain current.

III. DC OFFSET MODELING

Several factors contribute to the random offset voltage. Few of these are: mismatches in the input pair devices and in the active load devices, their threshold voltages and current gain factor. The placement of the devices also plays some role in estimation of mismatches. Out of these, threshold voltage and current gain factor are the dominant contributors [6, 7]. Therefore, the variance (σ^2) of threshold voltage (ΔV_{TH}) and current gain factor ($\Delta\beta/\beta$) is given by [6, 7]

$$\sigma^2(\Delta V_{TH}) = \frac{A_{VT}^2}{W.L} + S^2D^2 \tag{3}$$

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_{\beta}^2}{W.L} \tag{4}$$

A_{VT} is threshold process area proportionality parameter, A_β is technology dependent, D is the distance between two matched devices and S is process dependent parameter. Therefore, the drain current mismatch, valid in all regions of operation is given by [7]

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_{DS}}\right)^2 \sigma^2(\Delta V_{TH}) \tag{5}$$

Similarly, for the gate-to-source voltage is given by

$$\sigma^2(\Delta V_{GS}) = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \left(\frac{I_{DS}}{g_m}\right)^2 + \sigma^2(\Delta V_{TH}) \tag{6}$$

It has been reported that difference in threshold voltage contributes more to offset voltage than current gain [5, 7].

Dropping the distance factor from equation (3), and then using it along with equation (5) and (6), following equations are obtained

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right) = \left(\frac{g_m}{I_{DS}}\right)\frac{A_{VT}}{\sqrt{W.L}} \tag{7}$$

$$\sigma(\Delta V_{GS}) = \frac{A_{VT}}{\sqrt{W.L}} \tag{8}$$

Now, in case of differential amplifier (Fig.1), random input offset voltage is contributed by the mismatches in MN1, MN2 and MP1, MP2.Since, input differential pair is biased by the same current, only threshold voltage mismatch would contribute for the offset voltage. While in case of voltage biased current mirror, the offset voltage is multiplied by the current to transconductance ratio of input pair transistor.

Also the mismatches in W/L of input and load transistors contribute to the offset voltage [14].

Taking above facts into consideration, the expression for standard deviation of offset voltage can be written as,

$$\sigma(V_{OS}) = \sigma(\Delta V_{GS})_{MN1,2} + \left(\frac{I_{DS}}{g_m}\right)_{MN1,2}\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)_{MP1,2} + \left(\frac{I_{DS}}{g_m}\right)_{MN1,2}\left(\frac{\Delta\frac{W}{L_{MN1,2}}}{\frac{W}{L_{MN1,2}}} - \frac{\Delta\frac{W}{L_{MP1,2}}}{\frac{W}{L_{MP1,2}}}\right) \tag{9}$$

Using equations (7), (8) and (9), we get

$$\sigma(V_{OS}) = \frac{A_{VTNMOS}}{\sqrt{(W.L)_{MN1,2}}} + \left(\frac{I_{DS}}{g_m}\right)_{MN1,2}\left(\frac{g_m}{I_{DS}}\right)_{MP1,2} \times \frac{A_{VTPMOS}}{\sqrt{(W.L)_{MP1,2}}} + \left(\frac{I_{DS}}{g_m}\right)_{MN1,2}\left(\frac{\Delta\frac{W}{L_{MN1,2}}}{\frac{W}{L_{MN1,2}}} - \frac{\Delta\frac{W}{L_{MP1,2}}}{\frac{W}{L_{MP1,2}}}\right) \tag{10}$$

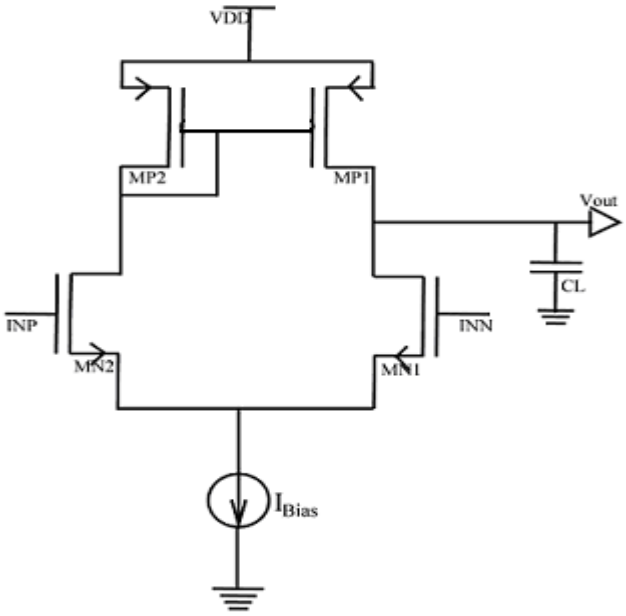

Fig. 1. Schematic Diagram of CMOS Differential Amplifier

From equation (10), we can model the offset voltage for the differential amplifier when the devices are operating in either saturation or subthreshold region.

Let us first consider the case, when both input pair and load devices are operating in saturation. In this case, we can minimize the offset voltage by choosing the appropriate values of dimensions and transconductance ratio of input pair and active load devices. In addition to this, it is to be noted that current to transconductance ratio in second term of equation (10), which shows the square root proportionality; and provides the higher value to contribute for offset.

Whiles in case of subthreshold region, the current is substantially small and transconductance shows a linear relationship with current. In that case, if the input pair devices are operated in subthreshold region, current to transconductance term due to input pair transistor in second term of equation (10) produces a significant reduction in offset voltage as compares to the saturation region. The active load devices are operated in saturation. If these are also operated in subthreshold region, they will cancel out the above reduction resulting in more offset voltage. Therefore, this is one of the primary reasons to operate the active load devices in saturation instead of weak inversion while working with subthreshold operation. In addition to this, in last term of equation (10) current to transconductance ratio term due to input pair devices is small and reduces the value of offset voltage compare to the case of saturation region of operation.

IV. Noise Minimization

The MOS devices exhibit higher noise level compared to their bipolar counterparts [16], therefore the noise performance is an important consideration for MOS amplifier. In case of MOS differential amplifier, the noise is contributed equally by all four devices, MN1, MN2 and MP1, MP2. The expression for the input referred noise for differential amplifier is given by equation [17],

$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_{MN1}} + \frac{2g_{MP1}}{2g_{MN1}^2}\right) + \frac{2K_N}{C_{ox}(W.L)_{MN1}.f} + \frac{2K_P}{C_{ox}(W.L)_{MP1}.f}\frac{g_{MP1}^2}{g_{MN1}^2} \tag{11}$$

k is Boltzmann constant, T is absolute temperature, K_N and K_P are the noise coefficient for NMOS and PMOS respectively and other symbols have their usual meaning.

From the above equation, it can be seen that noise performance of the differential amplifier can be improved by adjusting the transconductance ratios of input pair devices and active load devices. However, if input pair is biased in weak inversion region, it results in higher value of transconductance compared to saturation region, thereby reducing noise. Furthermore, in subthreshold region, the current flow is mainly due to diffusion and not due to drift, hence we have reduction in noise as in the case of bipolar device [13]. Although, choice of NMOS or PMOS in input pair is governed by system requirement but it is an important factor as PMOS devices display lower 1/f noise compared to NMOS [16].

V. Design Procedure

In subthreshold region of operation, MOSFET is biased at very low current (in range of 100 nA), it displays low bandwidth and slew rate. However, with current level near 1 μA, subthreshold operation may be achived [2]. This design has been done for 1 MHz gain bandwidth product, 1 μA bias current and 2 pF of load capacitance values.

$$Gain Bandwidth = \frac{g_{mMN1}}{C_L} \tag{12}$$

$$Gain = g_{mMN1}\left(r_{oMN1} \,//\, r_{oMP1}\right) \tag{13}$$

$$r_o = \frac{1}{\lambda I_D},$$

λ is channel length modulation parameter and has the different values in different region of operation for NMOS and PMOS devices.

For calculation of offset voltage, the expression for the offset voltage in equation (10), the third term is introduced due to the mismatches in W/L ratios and the distance between the input pair devices, which results in very small contribution. Ignoring this term, equation (10) can be written as,

$$\sigma(V_{OS}) = \frac{A_{VTNMOS}}{\sqrt{(W.L)MN1,2}} + \left(\frac{I_{DS}}{g_m}\right)_{MN1,2}\left(\frac{g_m}{I_{DS}}\right)_{MP1,2} \times \frac{A_{VTPMOS}}{\sqrt{(W.L)_{MP1,2}}} \tag{14}$$

In saturation region of operation, the well known value of (I_{DS}/g_m) is $(V_{GS} - V_{TH})/2$. Therefore, above equation takes the form,

$$\sigma(V_{OS}) = \frac{A_{VTNMOS}}{\sqrt{(W.L)MN1,2}} + \left(\frac{(V_{GS} - V_{th})_{MN1}}{(V_{GS} - V_{th})_{MP1}}\right) \times \frac{A_{VTPMOS}}{\sqrt{(W.L)_{MP1,2}}} \tag{15}$$

For subthreshold region of operation, putting the value of (I_{DS}/g_m) from equation (2) into (14), the expression for the subthreshold turns out to be

$$\sigma(V_{OS}) = \frac{A_{VTNMOS}}{\sqrt{(W.L)MN1,2}} + \left(\frac{2nV_T}{(V_{GS} - V_{th})_{MP1}}\right) \times \frac{A_{VTPMOS}}{\sqrt{(W.L)_{MP1,2}}} \tag{16}$$

Equation (16) provides the expression for the offset voltage in terms of design parameters: overdrive voltage and device dimensions for diff-amp, whose input devices are operating in subthreshold region. In equation (16), V_T is thermal voltage having value 26mV at room temperature, $(V_{GS} - V_T)$ is the overdrive voltage, which generally has the value in range of 100-200 mV and n is subthreshold slope having value in range of 1 to 2. The ratio of thermal voltage and overdrive voltage provides very low value compare to the overdrive voltages ratio as in equation (15). Due to this, a significant reduction has been exhibited in subthreshold region when compared with saturation region.

VI. Simulation Results

Although, we have given the design procedure for basic parameters, and the main motive of this work is to develop a formulation for the offset voltage in subthreshold region, analyze it for the optimized value and minimize the input referred noise.

TABLE I. *W/L* for Different Cases

Case		0.35 µm				0.18 µm			
		Saturation		Subthreshold		Saturation		Subthreshold	
		W (µ)	L (µ)	W (µ)	L (µ)	W (µ)	L (µ)	W (µ)	L (µ)
1	MN1	4	2	100	2	1	1	150	1
	MP1	12	2	12	2	3	1	3	1
2	MN1	8	4	200	4	2	2	300	2
	MP1	24	4	24	4	6	2	6	2
3	MN1	16	8	400	8	4	4	600	4
	MP1	48	8	48	8	12	4	12	4
4	MN1	32	16	800	16	8	8	1200	8
	MP1	96	16	96	16	24	8	24	8

Comparison has been done of the offset voltage and noise for different dimension of devices in saturation and subthreshold region in both 0.35 µm and 0.18 µm CMOS technology. We have taken four cases of different dimensions. We assume that MN1 and MN2 have same dimensions. Similarly, MP1 and MP2 have same dimensions.

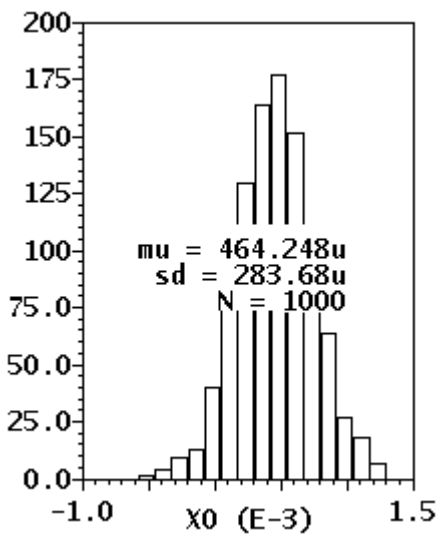

Fig. 2. Monte Carlo Histogram for offset voltage in 0.35 µm in subthreshold region

Fig. 2 and Fig. 3 display the Monte Carlo Simulation results of input offset voltage in subthreshold region for case4 and case3 for 0.35 µm and 0.18µm CMOS technology. These simulation results agree with first order calculation. The values of parameters, A_{VTNMOS} and $A_{VTPMOS,}$ have been taken from [18] and [19].

In order to verify the formulated method of offset voltage in subthreshold region, a comparison between calculated and simulated values has been shown in Table II. Also, the comparison for offset voltage in saturation region and subthreshold region has been displayed.

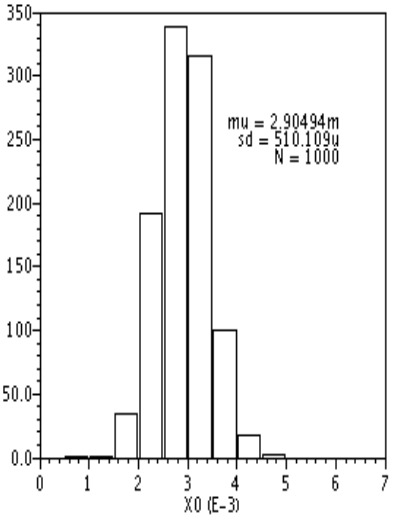

Fig. 3. Monte Carlo Histogram for Offset voltage in 0.18 µm in subthreshold region

TABLE II. Comparison for Offset Voltage

Case	0.35 µm V_{OS} (mV)				0.18 µm V_{OS} (mV)			
	Saturation		Subthreshold		Saturation		Subthreshold	
	Cal.	Sim.	Cal	Sim.	Cal	Sim.	Cal	Sim.
1	5.53	4.35	2.61	2.23	6.7	5.38	1.88	1.67
2	2.58	2.17	1..36	1.12	3.22	2.68	0.926	0.897
3	1.27	1.08	0.641	0.565	1.57	1.34	0.466	0.510
4	0.602	0.54	0.313	0.283	0.707	0.693	0.233	0.228

Analyzing, the values in Table II, we infer that the offset voltage formulation is in agreement with simulation data for subthreshold region of operation. In addition, to this, offset voltage has reduced significantly for subthreshold region in comparison to saturation region for both the technologies.

Simulation results for input referred noise in saturation and subthreshold region for the case 4 in 0.35 µm and 0.18 µm technologies have been shown in Fig. 4, Fig. 5 and Fig. 6, Fig. 7 respectively.

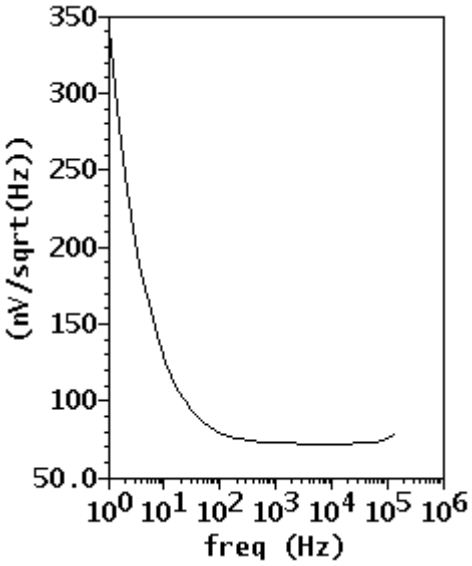

Fig. 4. Input Noise Performance of Diff-amp in Saturation for 0.35 µm

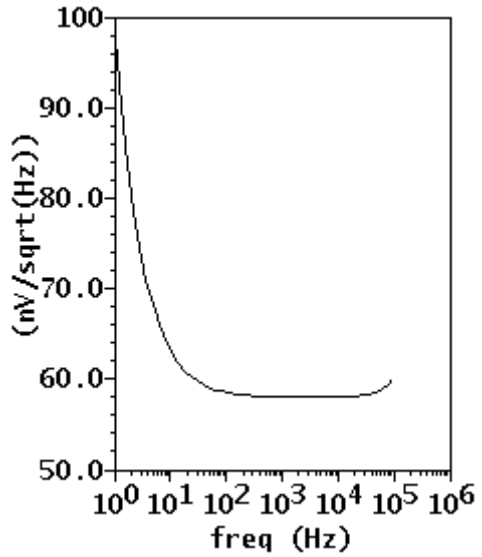

Fig. 5. Input Noise Performance of Diff-amp in subthreshold for 0.35µm

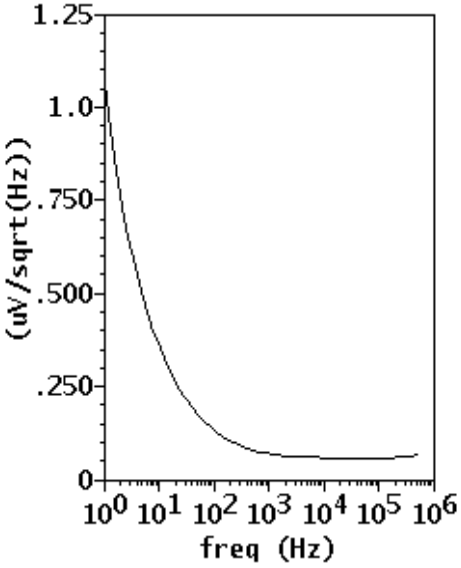

Fig. 6. Input Noise Performance of Diff-amp in Saturation for 0.18 µm

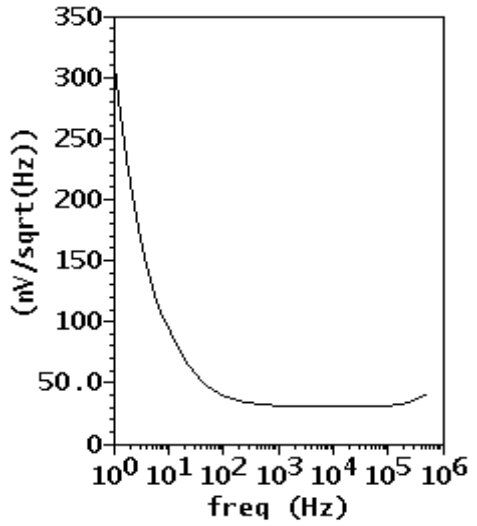

Fig. 7. Input Noise Performance of Diff-amp in Subthreshold for 0.18 µm

Table III provides the comparison for simulated results between saturation and subthreshold region for input noise at 10 Hz and 100 KHz in both the technologies.

Analysis of results from TABLE III indicates that the 1/f noise of differential amplifier leads to significant reduction in subthreshold region of operation.

TABLE III. Comparison of Input Noise for Saturation and Subthreshold at 10 Hz and 100 KHZ.

Case		0.35 µm V^2in (nV/√HZ)		0.18 µm V^2in (nV/√HZ)	
		Saturation	**Subthreshold**	**Saturation**	**Subthreshold**
1	10 HZ	1001.3	211.13	4001.20	984.24
	100KHz	79.79	57.88	82.23	32.39
2	10 HZ	462.65	115.61	1910.01	561.57
	100KHz	73.80	57.97	68.13	35.10
3	10 HZ	229.04	76.19	935.68	364.10
	100KHz	72.23	57.91	66.09	40.10
4	10 HZ	127.85	62.96	358.57	93.75
	100KHz	75.17	57.93	57.31	36.60

VII. CONCLUSION

The paper presents the DC offset modeling for CMOS diffrential amplifier in subthreshold region of operation. The formulation method has been verified with simulation results in two technologies. Finally, a methodology to optimize the input offset voltage and 1/f noise has been presented. To illustrate the advantage of the method, a detailed comparision of saturation region and subthreshold region operation diff-amp for offset voltage and 1/f noise has been done.

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