Generation and Annihilation of Process Induced Deep Level Defects in MOS Structures

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The deep-level traps in Si substrates induced during the processing of Ni/ SiO_2/n-Si have been investigated using deep level transient spectroscopy (DLTS). A deep level trap was detected at E_C - 0.49 eV, which was estimated to be introduced during high temperature thermal oxidation process. The trap position was found to shift to different energy levels (E_c-0.43 eV, E_c-0.46 eV and E_c-0.34eV) during annihilation process. The deep level traps completely annealed at 350°C. Significant reduction in trap density with a systematic increase in recombination life time and the substrate doping concentration as a function of isochronal annealing were observed. The relevant details are discussed in this paper.

Index Terms—**DLTS, Deep Levels, MOS, Oxidation, Process induced defects, Trap density.**

I. Introduction

The Process induced defects are of serious concern for modern sub-micron Si devices. As the technology leading to very large scale integration, millions of components are fabricated on a single chip. To ensure proper functioning of the chip, the fraction of the defective components must be smaller than 10^{-6} components/chip [1]. This implies that even a small number of defects may potentially cause a serious threat to the reliability which leads to failure of semiconductor devices. Semiconductor device processing includes large number of steps viz. oxidation, diffusion, ion implantation, metallization etc., which may lead to introduction of defects. Some of the steps which are associated with high temperature processing like thermal oxidation are found to generate dislocations in the silicon bulk [2][3]. With technological scaling of semiconductor devices, the processing steps tend to become more complicated and are likely to result in more process induced defects. Hence it becomes very necessary to identify such defects and to understand its behavior.

Several techniques like Electrically Detected Magnetic Resonance (EDMR), Electron Paramagnetic Resonance (EPR), Thermally Stimulated Current (TSC) and Thermally Stimulated Capacitance (TSCAP) are used in the characterization of defects in Si devices. In our present study, a more recent and widely used technique, Deep Level Transient Spectroscopy (DLTS), a capacitance transient thermal scanning technique was used to characterize the deep levels in the silicon band gap, as it overcomes the drawbacks of other conventional techniques like TSC and TSCAP in view of its better immunity to noise and surface channel leakage current. DLTS is sensitive (detects trap concentrations as less as 10^{-4} in order), spectroscopic (exhibits a peak for each trap detected) and allows to obtain parameters from either minority (positive peak in the spectral result) or majority carrier traps (negative peak). Easy and direct interpretation of experimental results obtained from DLTS makes it an interesting tool for defect analysis [4][5][6]

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II. Materials & Methods

A. Fabrication of MOS structure

The MOS capacitor structures were prepared in the clean room facilities at Central Electronics Engineering Research Institute (CEERI), Pilani. Structures were fabricated on Silicon wafer <100> oriented, n-type Phosphorous doped, 1.5 inch diameter and 220 microns thick. The sheet resistance was measured to be 0.20 - 0.22 Ω /□. The Si wafer was degreased for 5 min in boiling Tri-Chloro Ethylene, Acetone and Methanol consecutively. Standard cleaning procedures like RCA-I, RCA-II and piranha were followed to remove organic residues and metal ions from Si wafer. In case of RCA-I, the wafer was dipped in a solution of H_2O:H_2O_2:NH_4OH (5:1:1). In RCA-II the wafer was dipped in a solution of H_2O: HCL: H_2O_2 (6:1:1) and in Piranha wafer was dipped in H_2SO_4: H_2O_2 (7:1) solution. After each cleaning procedure the wafer was thoroughly cleaned with de-ionized water and dipped in HF for few seconds to remove native Oxides. Finally the wafer was again dipped in methanol and dried using nitrogen gun. The wafer was loaded into the oxidation furnace at 800˚C in N_2 ambient. The thermal oxide growth was done at 1050˚C in dry oxygen atmosphere for 40 min. The wafer was cooled at a rate of ~1˚C/sec in N_2 ambient and unloaded from the furnace at 800˚C. The oxide thickness was measured to be 82nm on Ellipsometer. Ni was selected for the Gate contact. Metallization for Gate was done under vacuum of 10^{-7} torr using Varian's e-beam metallization unit. Circular Ni dots with 2mm diameter were formed uniformly all over the wafer which was defined using metal mask. Silver was used to provide ohmic contact on the back side of the wafer.

B. DLTS Measurements

Since its introduction by Lang in 1974 deep-level transient spectroscopy has become a widely used method to investigate deep traps in semiconductors [7]. The DLTS system (IMS-2000) employed for the present study consists of a boxcar averager, a pulse generator, a thousand point digitizer, a voltage generator and a high speed capacitance meter. The

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pulse generator is capable of generating pulses with widths ranging from 100 ns to 10 s. The pulse height could be programmed from -12 V to +12 V. The boxcar averager is capable of generating seven rate windows. The time constants can be varied from 1 ms to 2 s. In the present study, DLTS spectra are recorded with a reverse bias of 5 V and pulse width of 20 ms applied between the Gate and the substrate. DLTS spectra were recorded for as processed MOS cap. The device was subjected to isochronal annealing for 30 mins at various temperatures (200°C, 250°C, 300°C, 350°C) respectively and the DLTS spectra were recorded for each annealing temperature. The trap concentration, activation energy and capture cross section of different deep levels were determined by DLTS spectra.

III. Result & Discussion

Fig.1. Shows the typical DLTS spectra for n-type Si-SiO_2 MOS structures before and after annealing at various temperatures.

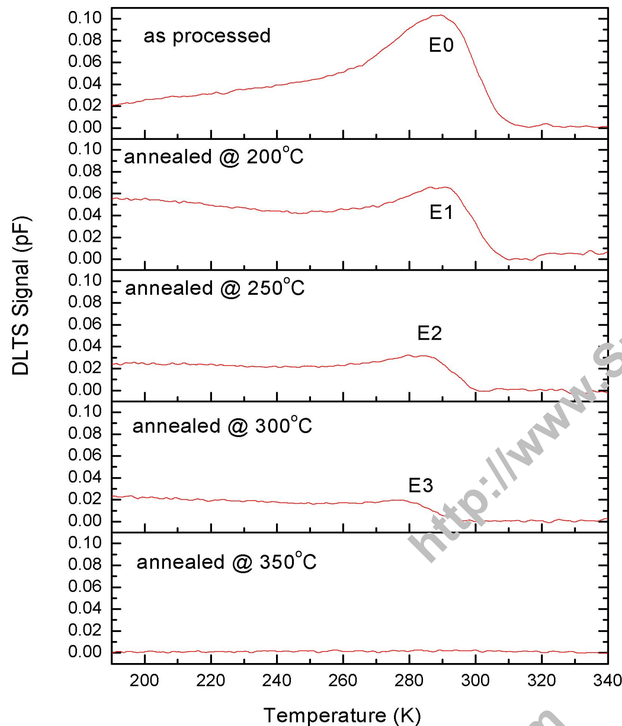

Fig.1. DLTS spectra of n-type Si-SiO_2 Structure before and after annealing

As one can see from the Fig.1, the DLTS spectrum of the as processed sample exhibits one peak at T=302K which corresponds to a deep level (E_0) with activation energy of E_C-0.49 eV in the forbidden gap of silicon. The capture cross section of 6.2 x 10^{-17} and a corresponding trap concentration of 1.10 x 10^{15} cm^{-3} were calculated from the measured data. This defect can be attributed to interstitial silicon or the self interstitial Si(i) caused due to oxidation of silicon samples [8][9]. After annealing the device at 200°C for 30 mins, the defect acquires a different energy level (E_1) with activation energy E_c-0.43 eV, capture cross section 6.96 x10^{-18} and a corresponding trap concentration of 7.15 x 10^{14} cm^{-3}. This defect found at a scanning temperature T=299K can be attributed to the Phosphorous Vacancy pair (V-P)whose origin may be because of carbon traces in Si [10]. The device was again annealed for 30 mins at 250°C and the defect peak was found at T=294K. This defect had an activation energy E_c-0.46 eV, capture cross section 4.49 x 10^{-17} and a corresponding trap concentration of 3.65 x 10^{14} cm^{-3} and is associated with vacancy related complexes (in our case phosphorous) [11][12]. Further annealing at 300°C creates a defect with still reduced trap concentration 1.62 x 10^{14} cm^{-3} at temperature T=288K . The activation energy of this defect was calculated to be E_c-0.34 eV and cross section 4.87 x 10^{-19}. This defect can be attributed to the multi-vacancy-oxygen (V_2O_2 or V_3O) defect [10][13]. No peaks were observed in the DLTS signal after annealing the device at 350°C. The significant reduction in the trap density due to annealing can be observed from Fig.2. The decreasing peak height in the DLTS signal is in direct relation with the reduction of trap density. The reducing trap densities is in conformal with the carrier life time which increases from 1.29 x 10^{-6} Secs to 1.44 x 10^{-3} Secs after annealing as shown in Fig.3. Appreciable increase in substrate doping concentration can also be observed from Fig.4. which increases from 8.86 x 10^{15} to 1.33 x 10^{16}

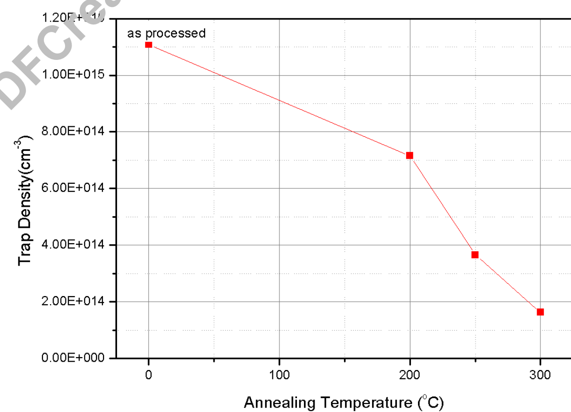

Fig.2. Density of traps measured after each annealing temperature

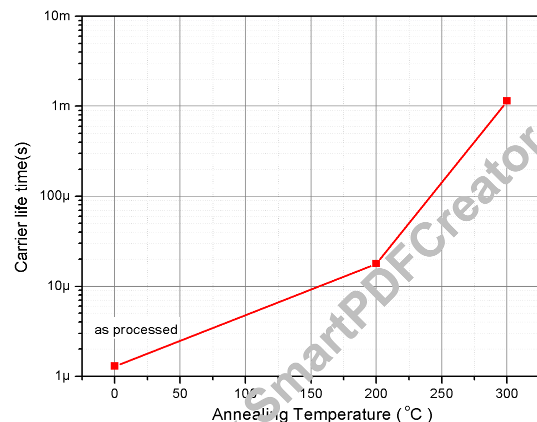

Fig.3. Carrier life time measured after each annealing temperature

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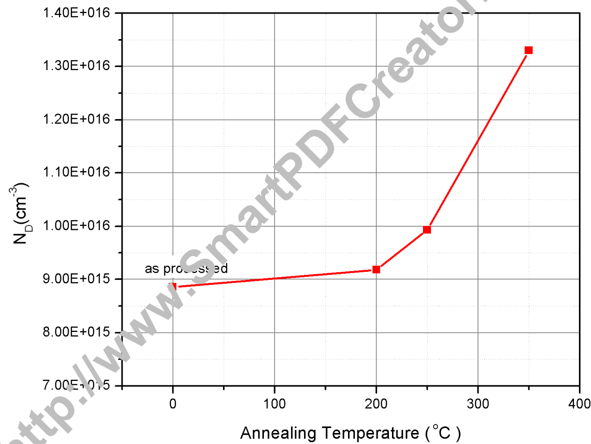

Fig.4. Substrate doping measured after each annealing temperature

IV. Conclusion

The DLTS data shows that deep level defects are introduced during processing of MOS structures. Four new energy levels are identified which is related to Silicon self interstitial, V-P and V-O complexes. The trap density is found to decrease with increase in annealing temperature. The recombination lifetime and substrate doping was calculated using the data acquired during measurement and is found to increase as a function of annealing temperature. The DLTS data showed no peaks after annealing the device at 350°C.

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