Mask Designing and Process Definition of Backside Contacted ISFET

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Abstract-
A fabrication method for Ion-Sensitive Field-Effect Transistor (ISFET) structures is proposed. In this approach, external electrical contacts to the n+ source and drain regions are made through individual cavities etched from the backside and the sidewalls isolation will be provided in the cavities and metallization covering the sidewalls. The FET structure will be constructed on the front face of the chip. The connections between the source and the drain diffusion and the back contacts will be achieved by diffusing impurities from both sides of the wafer. The front surface will have an insulating surface where the chemically active gate will be placed. The device will thus act as a chemical sensor. This will contrast with traditional ISFET devices where the gate and the contacts are placed on the front surface of the transistor. These sensors will be more compact, easily mounted and there encapsulation is much easier as compared to conventional chemical sensors. However, the fabrication technology will be more complex.

*Keywords-***ISFETs, Back contacts, Deep Diffusion**

I. INTRODUCTION

The concept of assembling of Ion Sensitive Field Effect Transistor (ISFET) structures with contact pads located at the back – passive side of the structure, facilitates considerably protection of the structure against chemically aggressive environment and makes exchange of the structure in field condition much easier. This approach, however, poses difficult technological requirements. To ensure the electrical connection throughout the silicon wafer thickness, around 500µm deep cavities will be formed to reach a close vicinity of the active side of the device followed by deep diffusion throughout the remaining silicon membrane. Next, this deep cavity will be effectively coated with continuous metal film which forms a contact pad to external connector. Coating and structuring of such 3-D structures requires special technological endeavors.

II. BACKGROUND

Forty two years ago, Bergveld introduced the first ion-sensitive field - effect transistor (ISFET) [1], which was used for ion concentration measurement as a function of electrical potential. In the past, many attempts have been made to achieve the desired isolation between the environment to which the ISFET is exposed and its associated electrical circuitry. There are various geometries, encapsulation approaches and mounting techniques have been proposed and developed [2-5]. The common aim of these developments was the production of chemical sensors that are low cost and reliable. Most of these devices were fabricated using a planar technology where the drain, the source and the gate, represented by the ion-sensitive area, are placed on the same face of the chip.

In analytical and biomedical applications, encapsulation is the major problem that has hindered the full impact of semiconductor chemical sensors and traditional ISFETs also suffer from this problem. Encapsulates often suffer from liftoff, allowing the aqueous electrolytic solution to touch the metallic contacts, producing a short circuit and the appearance of sizable leakage currents. Whenever a leakage occurs, the ISFET is no longer functional, and if it is used *in vivo*, it might be unsafe as well. Additionally, for ISFET to express its potential as an inexpensive sensor, encapsulation has to be an automatic process [6].

An ISFET structure featuring electrical contacts on the back – passive side of the transistor has a lengthened distance between the exposed gate and the encapsulated electrical connections. Thus, it produces a larger obstacle for the onset of leakage current. Furthermore, encapsulation is easier to automatize as less precision is required for the deposition of encapsulate materials. Micromachining techniques, based on the selective anisotropic etching of silicon, have been used to produce ISFETs with back electrical contacts. These efforts have been the subject of a review by Edwald et al [7].

A cavity etched on the back face of the chip provides electrical access to the drain and source diffusions. A free ion-sensing area is left on the front face of the chip. Micromachining of pits for back contacts presents several problems. A great depth of field is required in wafer aligners and other optical tools in order to focus the wafer surface and the pit bottoms simultaneously. The main anisotropic etchants that can be used are TMAH, hydrazine, ethylene-diamine-pyrocatechol (EDP) and potassium hydroxide (KOH) [8]. These chemicals pose several handling and safety problems [9]. Hydrazine is an explosive and hazardous substance. EDP is highly toxic and carcinonogenic. The potassium ions present in KOH solutions pose a grave pollution risk to clean-room facilities. These problems call for a separate etching facility apart from clean-room installations [10].

In the present paper , a novel technique is presented where back contacts will be achieved by deep diffusions, providing clean and flat surfaces on the device. It can be implemented in a standard silicon fabrication facility where planar technologies are used. No special separate facilities are required[11].

III. PRINCIPLE OF OPERATION

The schematic structure of an ISFET is shown in Fig1. It consists of a p-type Si substrate with two n-doped regions, source and drain, separated by a short channel, i.e. covered by the gate insulator. Typically the gate insulator is a SiO_2 layer or a double layer insulator of $SiO_2 – Si_3N_4$, $SiO_2 – Al_2O_3$ or $SiO_2 – Ta_2O_5$. The upper layer of these double insulator structures, i.e. Si_3N_4, Al_2O_3, Ta_2O_5, typically serve as a sensitive membrane for pH sensitive ISFETs[12].

For operation of an ISFET, the gate voltage, V_G, is applied by a reference electrode (e.g., Ag/AgCl electrode), which is also responsible for fixing the potential of the test solution (analyte). When a sufficiently positive bias potential is applied to the gate (with respect to the bulk silicon substrate), an n-type inversion layer is induced in the channel between source and drain. The magnitude of the drain current, I_D, will be determined by the effective electrical resistance of the surface inversion layer and the voltage, V_{DS}, that is applied between source and drain. The mechanism of operation of the ISFET can be described by the processes (charge carrier distribution) which take place in each phase and at the interfaces. The Flatband voltage, V_{FB}, the threshold voltage, V_T, and the drain current, I_D for an ISFET is given by[12] :-

$$V_{FB} = E_{ref} - \Psi_o + X_{sol} - (Ø_{Si}/q) - (Q_{SS} + Q_{OX})/Cox$$

$$V_T = V_{FB} - (Q_B / Cox) + 2\,Ø_F$$

$$I_D = \beta\,(V_{GS} - V_T - \tfrac{1}{2} V_{DS}).\,V_{DS}$$

Where, V_{FB} :- Flatband Voltage

E_{ref} :- Potential relative to vacuum

Ψ_o :- Difference between the potential of the oxide surface & bulk solution

X_{sol} :- Surface dipole potential of the solution

$Ø_M$:- Gate Metal Work Function

$Ø_{Si}$:- Si Work Function

Q_{SS} :- Surface state density at the Si surface

Q_{OX} :- Field Oxide Charge

Q_B :- Depletion Charge in the Si

$Ø_F$:- Fermi Potential

COX :- The gate insulator capacitance per unit area

$\beta = \mu\, W/L$

μ :- Mobility of the e- in the inversion layer

W /L :- Aspect ratio of the channel which affects the transconductance.

The potential Ψ_o can be calculated by the Nernst-Nikolsky equation or using a similar equation for ISFETs with a solution–insulator interface. In the case of a pH-sensitive ISFET, the gate insulator (typically Si3N4, Al2O3 or Ta2O5) senses the H+-ion concentration, generating an interface potential on the gate insulator. The pH response can be explained by the so-called site-binding theory. This model assumes that in contact with an aqueous solution, the surface of the gate insulator hydrolyses into ionisable sites (e.g., OH groups). These active sites are either able to bind or release hydrogen ions in a dynamic exchange process. Thus, their state changes with the pH of the surrounding analyte. According to the site-binding model, the pH dependence of the interface potential analyte/pH-sensitive gate insulator, Ψ_o, is given by the following equation[12]:

$$\Psi_o = 2.3(kT/q)[\,\beta /(\,\beta + 1)](pHpzc - pH)$$

Where, pHpzc (point of zero charge) is the pH value for which $\Psi_o = 0$

k :- Boltzmann constant

T :- Absolute temperature

B :- A parameter which reflects the chemical sensitivity of the gate insulator and is dependent on the density of surface

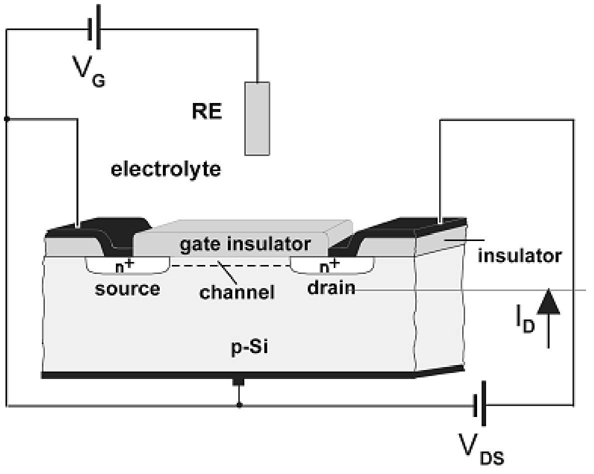

Fig.1 Structure of an ISFET, RE, reference electrode; V_G, gate voltage; V_{DS}, drain-source voltage; I_D, drain current.

IV. PROCESS SEQUENCE FOR BSC - ISFET FABRICATION

This process relates to chemical or electrochemical sensors based on Si FET technology for the measurement of hydrogen ions (pH) and activity of other ions in solution.

In the proposed ISFET structure, the electrical contacts to the source and drain regions will be made through individual cavities etched from the backside up to the source and drain regions with sidewall isolation provided in the holes, metallization covering the surface of sidewalls and extending to contact pads on the backside of the ISFET structure[13].

This ISFET will be fabricated by using a silicon substrate with a (100) orientation. An orientation dependent etch will be used to etch the cavities to the source and drain regions where the presence of an etch stop halts the etching process. A doped region will then be created in the sidewalls of the cavities to provide the isolation from the substrate and the metallization will then laid on the sidewalls to provide the external electrical contacts[14-16].

The preferred process for fabrication of an ISFET in accordance with the proposed structure is described below and the cross sectional view of an ISFET structure is shown in Fig2.

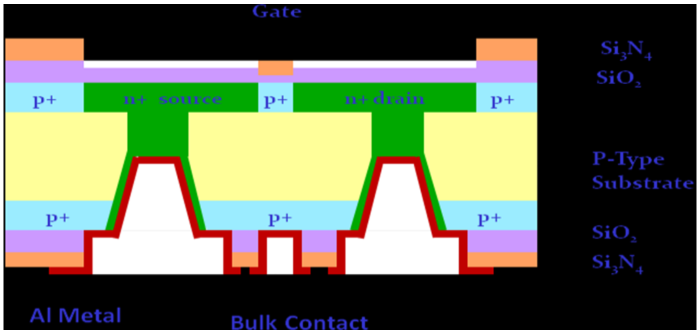

Fig.2 The cross sectional view of the BSC ISFET with source, drain & bulk Al contacts.

1. Start with a double polished P-type silicon wafer with a crystallographic orientation of (100), a resistivity of 10-20Ω-cm, a diameter of 4”, thickness of about 500-550 microns.
2. Grow a field oxide by thermal oxidation on both front and back side of the wafer to a thickness of about 1 micron at a temperature of about 1050℃ by following dry-wet-dry oxidation process for 30 minutes, 3 hours, and 30 minutes respectively.
3. Open window on the front side in the field oxide for the n+ deep diffusion by coating with photoresist except in the areas to be opened and then etching those areas.
4. For n+ deep diffusion, phosphorous doping will be done using oxygen with $POCl_3$ as a dopant and a source of phosphorous up-to a thickness of about 2 micron.
5. The drive-in step of the phosphorous diffusion process is carried out at 1000℃ for 90 minutes, which gives a depth of 4-6 micron n+ region.
6. Etch another window from the front side for defining field area for the p+ diffusion.
7. Protect the window opening from front side using photoresist and then again etch another window from the back side for the same purpose of field area definition.
8. p+ diffusion on both front and back sides will be done by chemical vapor deposition using BN source for boron at 1000℃ for 30 minutes.
9. Open window in the oxide from the front side for defining the field area by p+ diffusion.
10. Perform the p+ diffusion in the same way as described above.
11. The gate oxidation which is termed as trichloroethane oxidation is a type of dry oxidation process will be done for 90 minutes at the temperature of 1050℃ which produces a thickness of about 0.1micron.
12. After the gate oxidation process, the gate nitride layer which acts as an ion-sensitive membrane, will be grown by LPCVD technique for 20 minutes at a temperature of about 800℃ producing a thickness of about 0.07 micron.
13. Etch another window from the front side by RIE technique for gate formation, i.e., for defining source and drain.
14. Perform n+ diffusion for source and drain formation in the same way, as described above.
15. Etch another window from back-side for source and drain cavity formation again by using RIE technique.
16. Use TMAH solution for silicon etching which acts as an anisotropic etchant for cavity formation.
17. Produce n+ regions in the sidewalls of the cavities to isolate the p-type silicon substrate from the contacts to be formed. Thus source and drain regions are formed in the side walls of the etched cavities.
18. Drive-in diffusion is done into the sidewalls for 30 minutes at 1000℃.
19. Open window in the oxide from the back side for the electrical contact from the substrate.
20. Metallize the contact areas including the sidewalls of the cavities and associated areas on the back as contact pads for connection of the electrical circuitry to the source, drain and the substrate regions.

The proposed design comprises 8 photolithographic levels and the mask designing of the proposed design is done using L-Edit version 8.30. The complete mask layout is shown below in Fig.3.

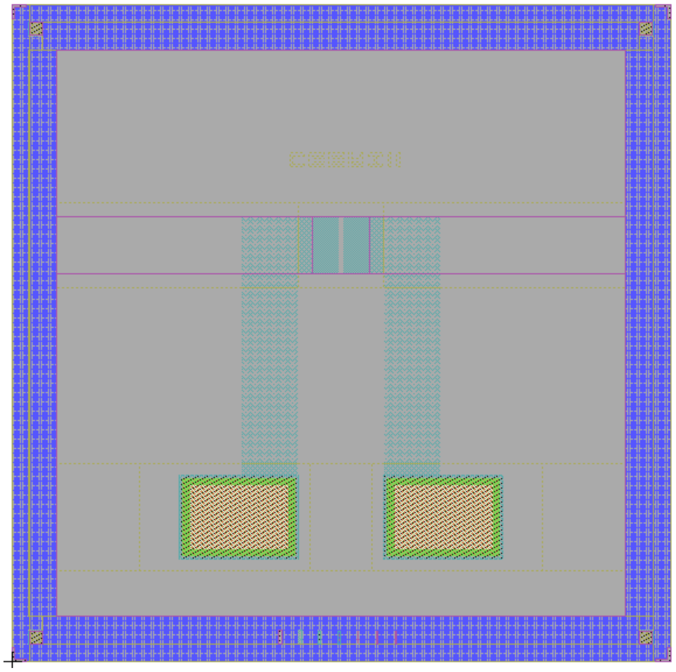

Fig.3 Combined Photo-mask showing the final pattern

V. CONCLUSIONS

The new design of an Ion Sensitive Field Effect Transistor (ISFET) having electrical connections at the back-passive side of the chip has been planned using a standard planar technology in which the back contacts would be formed using deep diffusion technique. These chemical sensors will overcome the problem of encapsulation that hindered the potential of traditional chemical sensors having all electrical connections of source, drain and gate on the front face of the chip. The new chemical sensors will be easier to encapsulate, more reliable and more compact however, the technology involved in its fabrication is more complex.

VI. ACKNOWLEDGEMENTS

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