Design of a 10-bit, 5 Ms/S Pipelined ADC for CMOS Image Sensor

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Abstract:

In this paper design of a 10bit, 5MS/s pipelined ADC suitable for chip level integration of CMOS image sensors has been attempted. The designed pipeline ADC is simulated in 3.3 V, double poly, triple metal 0.35 µm Austria Microsystems process. The maximum DNL and INL of the designed pipeline ADC are -1/+0.5LSB and -2.5/+1.75LSB respectively. The dynamic input range of the ADC is 3 V. The designed ADC eliminates the need of front end S/H circuit, thereby reducing the chip area and power. The designed pipeline ADC consumes a power of 40mW and chip area of only 0.49 mm^2. The offset cancellation of the S/H circuit and the Multiplying Digital-to-Analog circuit (MDAC) are done by the use of a simple offset cancellation switch.

Index: CMOS image Sensor, pipeline, ADC, flip-around, Sample-and-Hold

1. Introduction:

Modern multimedia applications starting from camcorder to video digital cameras demand the integration of ADCs and CMOS-based image sensor on a single chip. CMOS-based image sensor consists of a matrix of pixels depending on the required resolution of the image. There are different approaches of pixel implementation in CMOS technology such as passive pixel, active pixel etc. [1]. The development of active pixel sensors made the integration of image sensor and the read out circuit possible on a single chip i.e. camera-on-chip [1]. Due to modern CMOS technology the integration of image sensor along with the read out circuit leads to low cost, low power and low voltage camera-on-chip. Camera-on-chip requires on chip analog-to-digital converter with 8-10 bit resolution, less power consumption, and with lesser silicon area. The minimum required resolution of on-chip ADC is 8-bit with differential nonlinearity and integration nonlinearity as low as possible so as not to introduce distortion in the image. The power consumption of the ADC should be less than 100mW to avoid the introduction of hot spot [1]. There are different approaches for on chip integration of ADC like pixel level, column parallel level and finally the chip level [1-2]. Pixel level approach requires low speed ADC as each pixel is associated with a separate ADC, where as column parallel approach require medium speed ADCs as each ADC is allocated for one or several columns of pixels, But the chip level approach needs only one high speed ADC for the whole pixel array[1]. Due to reduced mismatch concerns, chip level integration is preferred over the other two types of integration [2]. For image processing application the on chip ADC must support a range of video rate of 0.92 MS/s for a 320x288 format sensor operating at 10 frames/s to 55.3 MS/s for a 1280x720 format sensor operating at 60 frames/s[1]. Requirement of such kind of video

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rate ADCs lead to pipelined ADC architecture because of its relatively lesser area and low power consumption over other ADCs. One such kind of video rate pipelined ADC with sampling rate of 6.3 MS/s and a resolution of 12-bit is reported in [2] for a CMOS image sensor in 0.35μm technology. The reported ADC [2] consumes a power of 50mW and relatively large area of 2.6 mm^2. Switch charge injection induced offsets and the offset of the Operational Amplifier (Op-Amp) puts a limitation in the design of high accuracy pipeline ADCs. One way of getting the accurate ADCs is to use digital calibration techniques [3-6]. The problem associated with the digital calibration techniques are higher power consumption with more silicon area and higher design complexity. Another solution is correlated double sampling (CDS) technique [7-8]. The problem with the CDS technique is its design complexity and the need of an extra clock phase along with the conventional two phase non overlapping clock for switched capacitor circuit. This extra clock puts a limitation on the speed of the data converter. However, for not losing the speed of data converters in the case of CDS technique, one need to chose for Op-Amp with lesser settling time which in return increases the power consumption due to higher current requirements. In the proposed architecture, the traditional pipelined architecture [9] along with an offset cancellation switch is used which cancels the offset due to both Op-Amp and switches. Compared to CDS technique, in the proposed design an extra clock phase is not used for offset cancellation which would otherwise put a limitation on ADC speed. Traditional approach of implementing the pipelined ADC along with an offset cancellation switch make the design simple without losing the benefits of low power, low silicon area, and high speed. The elimination of front end S/H leads to reduction in silicon area and power consumption. Proposed design works at a sampling frequency of 5MS/s with a resolution of 10bit. It occupies 0.49 mm^2 of silicon area, much less than reported in [2] and consumes 40 mW of power.

The working of the proposed pipelined ADC architecture is described in section-2. Section-3 deals with the working principle of S/H and residue Amplifier. Section-4 describes the comparator design and simulation results are discussed in section-5, finally conclusion is given in section-6.

2. Working principle of proposed pipelined ADC:

Proposed pipelined ADC is based on the traditional pipelined architecture [9] which is shown in figure-1. The pipelined ADC consists of several cascaded stages of 1-bit ADCs depending on the required resolution. In the present case the required resolution is 10 bit, hence ten 1-bit stages are cascaded. The pipeline ADC works with two phase non overlapping clocks shown in figure-1. In the first clock phase input signal is sampled to the Sample Hold circuit (S/H) of first stage. In the second clock phase S/H circuit holds the sampled value and the comparator produces a digital output of 0 or 1 based on the held input analog signal value. In the same clock phase, the residue amplifier passes on the output to the second stage. The output of the residue amplifier is decided by the pipelined ADC algorithm as follows:

If the comparator output is '1' then the residue amplifier output is equal to *(Vref-2Vin)* or else *2Vin.*

The motto behind the use of residue amplifier is to keep the signal constant and allow the same reference throughout the pipeline stages. The inherent problem in the traditional pipelined architecture is that the error from the first stage gets multiplied by a factor of two in subsequent stages. So, the error from the first stage must be within ½ LSB so as not to lose an LSB from the final ADC digital output. This ½ LSB includes the error due to: (i) the two S/H amplifiers, one at the starting of the first stage (front end S/H) and the second at the starting of second stage (ii) the residue amplifier of the first stage. Therefore, the errors from S/H and the residue amplifier must individually be within 1/6 LSB. For such an accurate S/H amplifier, Op-Amp must have a very small settling time with minimum offset due to gain error. Reduction of gain error require increase of gain and hence reduction of bandwidth. This will eventually reduce the speed of operation. Hence, to get rid of the gain offset errors without sacrificing the speed advantage of pipelined ADC, the best way is to eliminate the front end S/H circuit. Elimination of S/H front end can also reduce a significant amount of power and the input referred noise [10]. Such type of implementation are reported in [10-11] for achieving low power. The requirement of a front end S/H is to provide a stable dc input to the following stages. Basically, the purpose is to provide both residue amplifier and the comparator with a stable dc signal so that the two parallel paths see the same input signal regardless of their circuit implementation. Figure-2 shows the situation when front end S/H circuit is eliminated. As it can be seen from figure-2 there is a timing skew or phase mismatch between the passive switch capacitor sampler and the first stage comparator (A/D). Hence, this phase mismatch causes a dynamic (frequency dependent) comparator offset that can cause nonlinearity [12-13]. To compensate for the above dynamic offset, 1.5 bit per stage or digital redundancy is a well known technique [10-11], but the digital redundancy will increase the no. of comparators [14] which will lead to more power consumption and large silicon area. Another way of accommodating the above dynamic error is to increase the dynamic range of the input. In the proposed design the dynamic range of ADC has been increased. Elimination of front end S/H requires a single switched capacitor circuit known as Multiplying Digital to Analog Converter (MDAC) which integrates the S/H, subtraction, and residue gain functions [15]. The MDAC is shown in figure-3. Moreover, the comparator has to be chosen which has an integrated S/H circuit. So, in the proposed design, inverter based switched capacitor comparator is chosen, details of which are given in section-4. Both MDAC and the comparator sample the input signal in the first clock phase as shown in figure-4. In the second clock phase, the comparator compares the sampled input voltage with the reference voltage and the MDAC gives an output according to pipeline ADC algorithm as already described. As shown in figure-4, the width of the clock phase PHI1 is decided by: (i) the comparison time of the comparator (ii) the time taken by the residue amplifier to give its output. The two phase non overlapping clocks along with the carried out operations during their time period are shown in figure-4. In the design the propagation delay of the compactor is15ns while the worst case time required by the residue amplifier is 65ns. So, the total requirement of the time can easily be accommodated within the available time of 100ns for our 5 MS/s pipelined ADC. After the elimination of front end S/H amplifier, still there is a need to deal with the errors from the MDAC of the first stage and the S/H at the starting of the second stage. The main source of error from MDAC and the S/H amplifier is due the Op-Amps

and switches. As it is well known that the dc output offset voltage of the two stage Op-Amp is around 10-15mV, there is a need to go for a technique which can reduce the offset errors.CDS technique [7] is used to reduce the offset error induced by the Op-Amp. However, the problem with the CDS technique lies in the requirement of an extra clock phase for cancellation of the offset which again puts a limitation on the speed of the ADC. So, in the design a simple offset cancellation switch is used in both S/H and MDAC to reduce the offset errors. The finite gain of the Op-Amp also induces an error in the S/H and the MDAC. The error due to the finite gain of the Op-Amp can be given by the following equation [16]:

$$V_{err} = V_{ref} / (A_0) \text{ ---------- } (1)$$

Where β is the feedback factor, V_{ref} is the reference voltage which determines the signal range; A_0 is the open loop dc gain of Op-Amp. As it has already been discussed that the maximum allowable error is *0.5 LSB*, the gain can be derived from equation (1) as:

$$A_0 = V_{ref} / (\beta * 0.5LSB) \text{ ---------- } (2)$$

$$A_0 = V_{ref} / (\beta * (V_{ref} / 2^{N+1})) \text{ ---------- } (3)$$

Where, N is the no of bits to be resolved by the ADC
Assuming the feedback factor β=1
We have

$$Ao >= 2^{N+1} \text{ ---------- } (4)$$

So, from equation (4) it can be seen that the gain of the amplifier should be greater than 66dB for a 10bit pipeline ADC. So, a traditional miller compensated two stage amplifier is chosen to achieve the required gain [17]. In the proposed design, simple transmission gate switches are used in between the signal path and the sampling capacitor. The on resistances of the switches are chosen depending on the sampling frequency of ADC. The offset due to the charge injection of the switches are also reduced by the offset cancellation switch.

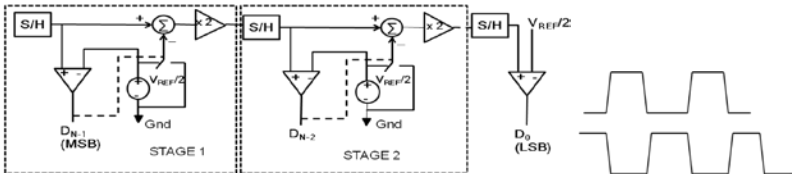


Figure1: Traditional pipeline ADC

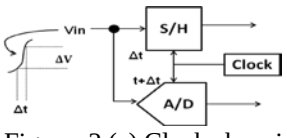
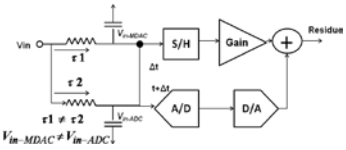


Figure: 2 (a) Clock skew in the front end S/H [12]



(b) Parallel signal paths showing the RC combination [13]

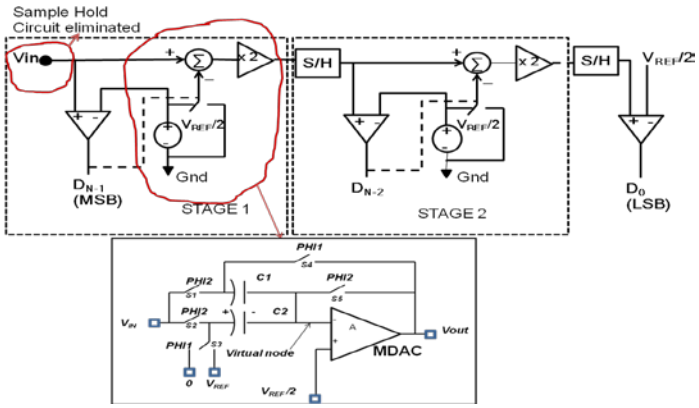


Figure 3: Pipeline ADC without front end S/H

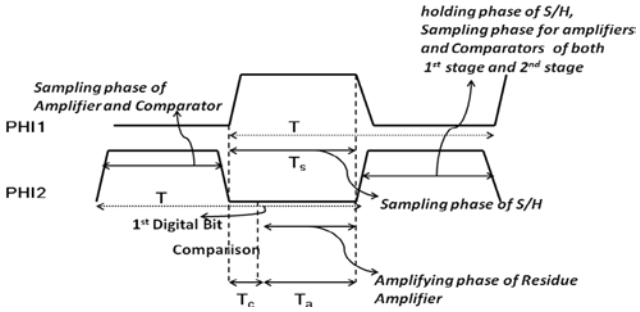


Figure 4: Two phase non-overlapping clock with operation sequence of pipeline stages

3. Working of Sample Hold(S/H) circuit:

As discussed in Section-2 the accuracy of the S/H circuit has to be increased. In contrast to conventional complex S/H circuits for achieving our specifications, a relatively simpler circuit [18] is used. The architecture of the S/H circuit is shown in figure-5. Conventional S/H architectures are based on either charge transfer [19] or flip-around [20] architectures. In either of the architectures a very precise and high performance amplifier is required [19-20]. Otherwise, in hold mode, dc gain limitation of Op-Amp will create an offset at the output of S/H circuit. Similarly, Phase Margin (PM) and Gain Band-Width (GBW) of Op-Amp will limit the overall frequency response of S/H circuit. Consider the macro-model of a S/H circuit shown in figure-6(a).Mathematically settling time of S/H circuit with capacitor in feedback path can be expressed as in equation below [18].

$$V_o(t) = V_o(t_o) - \frac{\alpha V_i}{1 + \frac{1}{\beta A_V}}\left[1 - e^{-WGBWt}\right] \quad \text{(5)}$$

$V_0(t)$ is the output voltage of the system in time domain.

Where $W_{GBW} = \frac{\beta_{gm}}{C_{tot}}$

α**=1** (for well matched capacitor)
β= *feed-back factor*
$A_v = g_m / g_0$ *(open loop dc gain)*

Transient response of the macro-model is shown in figure-6(b). The major factor affecting the gain error is the open-loop dc gain of the amplifier or the feedback factor "***β***". The previous reported work [19] is based on design of high open loop dc gain amplifier, as the feedback factor is considerably small. In flip-around architecture, the feedback factor is enhanced but still it requires a high gain amplifier with good phase margin [20]. In the current work an offset compensating switch is used across the amplifier to reduce the gain error during the sample mode. The compensating switch channel impedance is modified to maximize the feed-back factor of switch in sample mode. In the mean while, the input and output offset occurring across the amplifier is also taken care by the switch. The performance parameters of the amplifier are given in table-I. The amplifier used in this S/H is a well known two stage miller capacitor compensated amplifier [17].The details of the switch and S/H circuit can be found in [18]. The simulation results of the S/H circuit are shown in figure-7. The transient simulation of S/H is shown in figure-7(a). Monte Carlo simulation of the S/H circuit is shown in figure-7(b). In figure-7(b), output of a random input is shown. In the X-axis random voltages of input are shown and they are numbered 1 to 16 and the corresponding output voltages are shown in Y-axis. The maximum and minimum deviation of sampled voltage from the input voltage is shown by output voltage (1) and output voltage (2). Monte Carlo results show a maximum variation of 2 mV in output voltage.

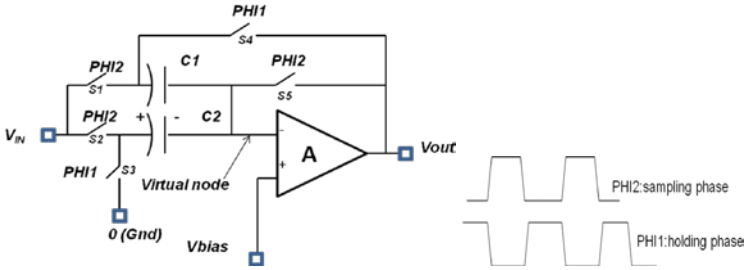


Figure:5 Architecture of S/H

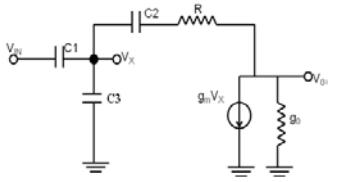


Figure:6(a) Macro model of a S/H Circuit

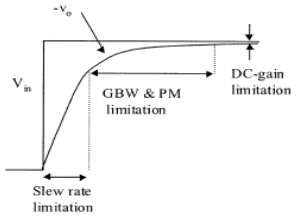


Figure:6(b) Transient response of the Macromodel

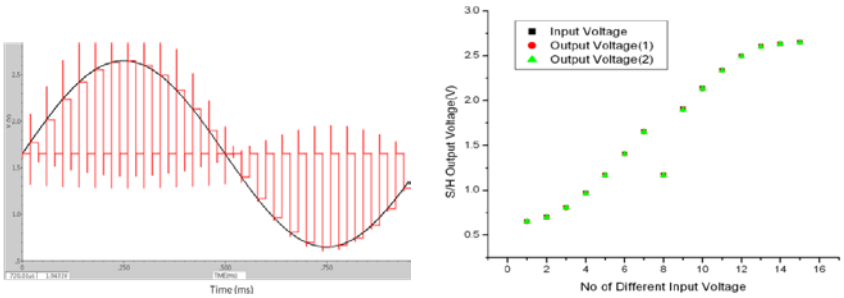


Figure:7(a) Transient Analysis of S/H (b) Monte Carlo Analysis Result of S/H

Table I: OpAmp parameters

Op-Amp Parameters	**Value**
Dc Gain	*75 dB*
Phase Margin	*65°*
Slew Rate	*8 V/µsec*
W_{3dB}	*1KHz*
UGB	*16MHz*
Output Impedance	*3KΩ*

The values of the capacitors of S/H are appropriately selected so that voltage transfer is not degraded because of process mismatch and the charge retaining ability. As a larger capacitor would degrade the settling time due to the loading effect on the amplifier, the capacitor is chosen just above the value of kT/C [thermal noise limitation]. The principle of offset cancellation in case of MDAC is same as S/H circuit.

4. Working of Comparator:

Pipeline ADCs are widely used due to their excellent performance at high speed. So, the digital bit producing circuit i.e. comparator must operate at high frequency. The simplest comparator architecture available is regenerative cross-coupled inverters [21]. This architecture is not suitable for high resolution application due to its large offset voltage. Hence, several pre-amplifier stages are placed before regenerative latch to minimize the offset and increase the accuracy during comparison. This increases the power consumption and raises the issue of stability [22]. Thus, in the proposed pipeline ADC the inverter based dynamic comparator [23] is used. The inverter based dynamic comparator is shown in the figure-8. This architecture is chosen because of its high speed of operation. It also eliminates the need of S/H circuit at the 1st stage of the pipelined ADC. As it can be seen from figure-8 that the comparator works in two phase non overlapping clock (figure-3). In the first clock phase switch s1 and s3 are closed and appropriate charges are stored in 'C'. In the next phase s1 and s3 are opened and s2 is closed. Writing down the appropriate charge transfer equations and using charge conservation principle, the voltage at the input of the inverter in amplifying mode can be written as

Vinv = (VREF – VIN) + VTH ---------- (8)

Where, ***VREF*** is the reference voltage of comparator, ***VIN*** is the input signal voltage, ***VTH*** is the logic threshold of the inverter and ***Vinv*** is the voltage at the input of the inverter ***inv1*** in amplifying mode.

As the gain of the amplifier is not much to give a full logic swing either 0 or VDD (supply voltage), two more inverters at the output of the first inverter are cascaded as shown in figure-8. Finally, the latch is used to latch the digital output. The inverter based dynamic comparator gives a resolution of 2mV and a typical propagation delay of 16 ns. The AC Small signal analysis of the inverter is shown in figure-9(a) which shows a gain of around 35dB over a wide range of frequency of 90 MHz. The Monte Carlo analysis of the inverter based comparator is shown in figure-9(b) which shows an average variation of 5ns (marked by two lines).

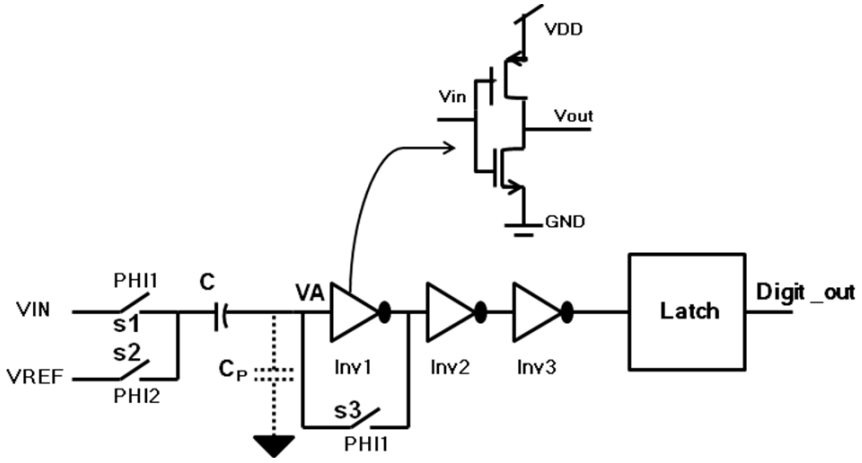


Figure8: Inverter based dynamic comparator

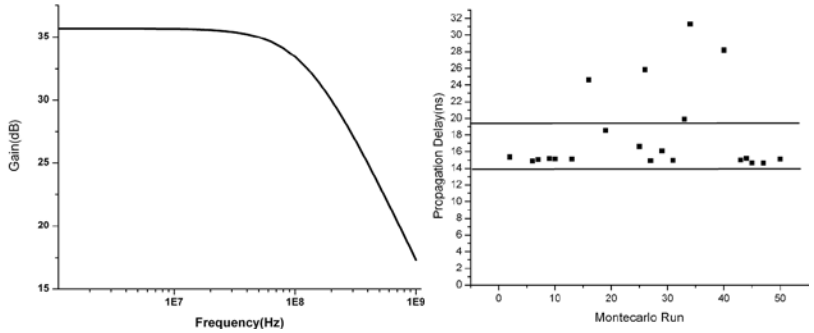


Figure: 9(a) AC analysis of inverter in amplifying mode (b) Monte Carlo analysis result

5. Simulation results:

The designed 10 bit pipeline ADC is simulated in 0.35µm Austria Microsystems for static characteristics like INL, DNL, along with the dynamic characteristics

SNR, SINAD etc. The DNL and INL simulation are done with the help of veriloga code. The veriloga code is based on the histogram method of testing INL and DNL [24]. The DNL and INL plots of the 10 bit pipelined ADC are shown in figure-10(a) & (b) respectively. The maximum DNL is -1 LSB, whereas the maximum INL is -2.5LSB. The dynamic characteristics of the ADC are obtained by performing transient noise simulation in cadence environment with the help of ideal DAC implemented in veriloga code. Transient noise analysis is carried out with a sinusoidal input of 4.883 KHz to the ADC with a sampling frequency of 5MS/s. Finally, the FFT analysis is done on the output from the ideal DAC with the help of Mat lab to find the dynamic characteristics of the ADC. The FFT analysis plot is as shown in the figure-11. The following parameters of the ADC are obtained from the FFT analysis: SNR = 64dB, SINAD=74.24, SFDR=78.36dB. Table.1 shows the comparison of different parameters of our designed ADC with the ADC designed in [2]. The comparison results show that our designed ADC can be used in CMOS sensor applications. The power consumption of the designed pipeline ADC is found to be 40mW, which is 20% less than in [2].The layout of the designed pipelined ADC is shown in figure-12. The layout occupies an area of 0.49mm^2, which is a huge reduction as far as silicon area usage is concerned.

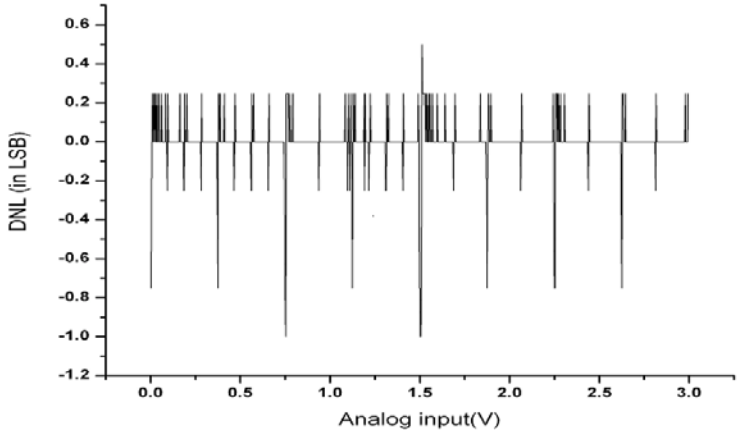
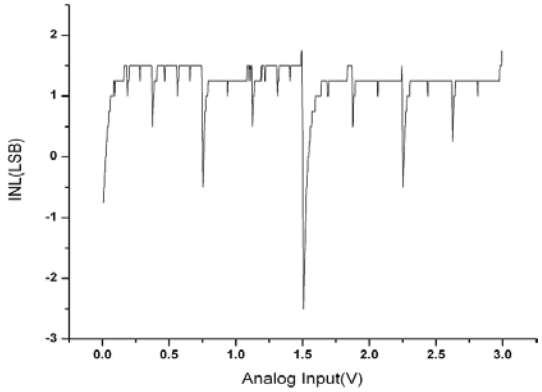


Figure: 10(a) DNL plot of the designed pipeline ADC



(b) INL plot of the designed pipeline ADC

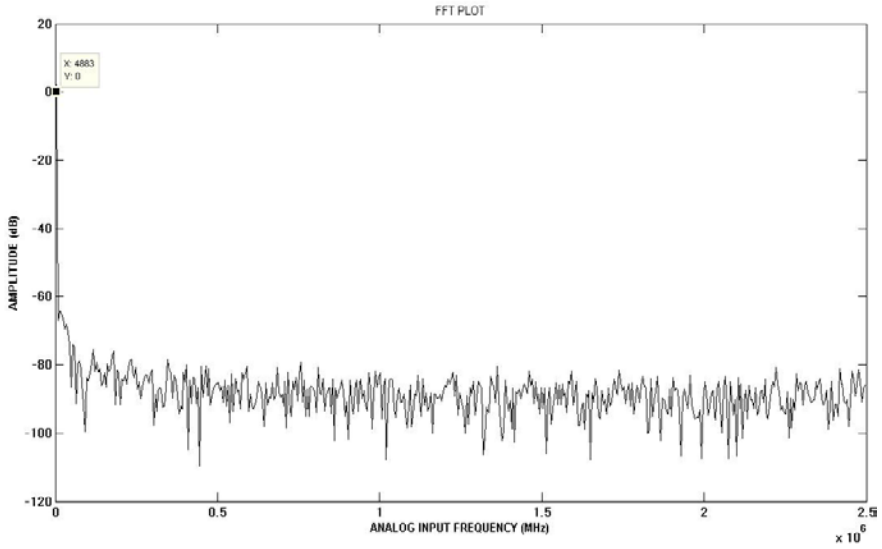


Figure: 11 FFT analysis of the designed pipeline ADC

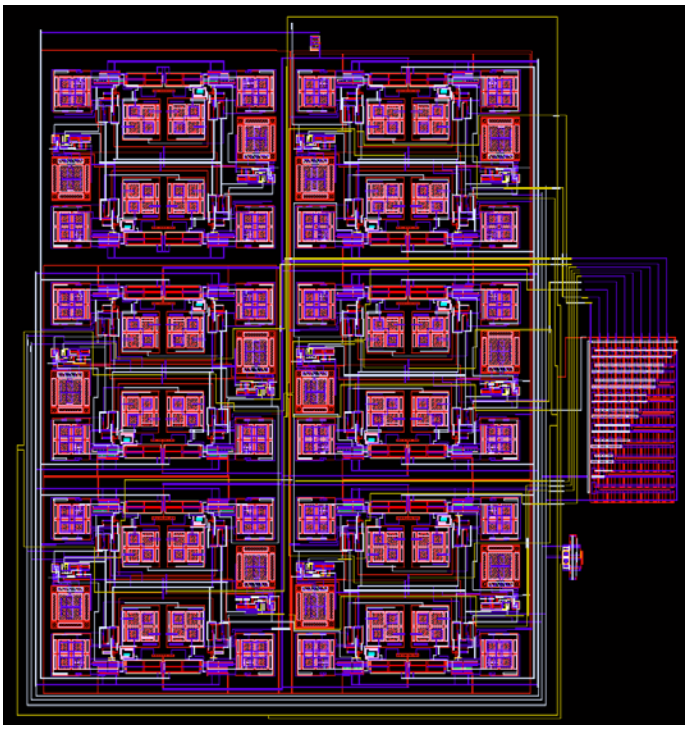


Figure: 12 Layout of the designed 10-bit pipeline ADC

Table II: comparison of the designed pipeline ADC in this paper with the one in reference [2]

ADC Parameter	Pipeline ADC [2]	Pipeline ADC[This Paper]
Technology	*0.35 µm*	*0.35µm*
Supply Voltage (V)	*3.3*	*3.3*
Resolution (No. of bits)	*12*	*10*
DNL (LSB)	*0.8*	*1*
INL (LSB)	*4.2*	*2.5*
Input Dynamic Range (V)	*±2*	*3*
Chip area (mm^2)	*2.16*	*0.49*
Power Dissipation (mW)	*50*	*40*

VI. Conclusion

An area efficient 10 bit pipelined ADC with offset compensating switch has been designed. This is very much suitable for the chip level integration of CMOS image sensor. The total occupied chip area by the designed chip is $0.49mm^2$. The total power consumed by the chip is 40mW. The Further reduction of power without losing speed can be achieved by reducing the bias currents of the amplifiers i.e. implementation of low power amplifiers.

References:

1. E.R. Fossum, "CMOS image sensors:Electronic camera-on-a-chip," in IEEE IEDM Tech. Dig, pp. 17-25,1995.
2. S. Hamami, L. Fleshel, O. Yadid-Pecht, "CMOS image sensor employing 3.3V 12bit 6.3 MS/s pipelined ADC", ScienceDirect Journal on Sensors and Actuators, pp.119-125,Jul-2006.
3. S.Lee and B.Song, "Digital-domain calibration of multi-step analog-to-digital converter," IEEE J. Solid-State Circuits,Vol.27,pp.1679-1688,Dec.1992.
4. A. Karanicolas and H.Lee, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC,"IEEE J. Solid-State Circuits,Vol.28,pp.1207-1215,Dec.1993.
5. H.Lee, "A 12-b 600ks/s digitally self-calibrated pipelined algorithmic ADC," IEEE J. Solid-State Circuits,Vol.29,pp.509-515,Apr-1994.
6. J. Ming and S.Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," IEEE J. Solid-State Circuits,Vol.36,pp.1489-1497,Oct-2001.
7. C. Enz and G. Temes, "Circuit techniques for reducing the effects of opamp imperfections: Autozeroing, correlated double sampling and chopper stabilization," proc. IEEE, pp.1584-1614, Nov.1996.
8. J. Li, Un-Ku Moon, "A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique", IEEE J. of Solid-State Circuits, Vol.39,pp.1468-1476,Sept-2004.
9. R. Jacob Baker, H. W. Li, D.E.Boyce, "CMOS Circuit Design,Layout,and Simulation", IEEE Press series on Microelectronic Systems, 2005.
10. A. M. Ali,C. Dillon, R. Sneed,A.S.Morgan,S. Bardsley,J. Kornblum,L. Wu, "A 14-bit 125 MS/s IF/RF Sampling Pipelined ADC With 100 dB SFDR

and 50 fs Jitter",IEEE J. of Solid-State Circuits, Vol.41, pp. 1846-1855, Aug-2006.
11. K. Gulati, M.S. Peng, A. Pulincherry, C. E. Munoz, M. Lugin, A. R. Bugeja,J. Li,A.P. Chandrakasan, "A Highly Integrated CMOS Analog Baseband Transceiver With 180 MSPS 13-bit Pipelined CMOS ADC and Dual 12-bit DACs", IEEE J. of Solid-State Circuits, Vol.41,pp.1856-1866,Aug-2006.
12. Yun Chiu, Paul R. Gray, B.Nicolic, "A 14-b 12-MS/s CMOS pipeline ADC with Over 100-dB SFDR", IEEE J. of Solid-State Circuits,Vol. 39,pp.2139-2151,Dec-2004.
13. Imran Ahmed, David A. johns, "A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold", IEEE J. of Solid-State Circuits,Vol.43,pp.1638-1647,Jul-2008.
14. S.H.Lewis,H.SottFetterman,G.F.Gross, R.Ramachandran,T.R.Viswanathan, "A 10-b 20-Msample/s Analog-to-Digital Converter,IEEE J. of Solid-State Circuits, Vol.27,pp-351-358,Mar-1992.
15. Joseph M. Ingino,Bruce A. Wooley, "A continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter",IEEE J. Solid-State Circuits,Vol. 33,pp.1920-1930,Dec.1998.
16. Ke Liu, H. Yang, "Optimum Design of A Fully Differential 12bit 100MS/s Sample and Hold Module with over 77dB SFDR", ASICON'07 on ASIC,pp 442-445,Oct-2007.
17. Gray,Hurst,Lewis,Meyer, " Analysis and Design of Analog Integrated Circuits", Wiley Student edition,2005.
18. M. santosh, Kanhu Ch. Behera, S.C.Bose, " Design of Pseudo Flip-around Sample-hold circuit for 10-bit, 5Msample/sec pipeline ADC", International conference on Emerging Trends in Electronic and Photonic Devices and Systems,pp.103-106 Dec-2009.
19. Lewis S, Gray P R, "A pipeline 5-Msample/s 9-bit analog-to-digital converter," IEEE J. of Solid- State Circuits, Vol.22, pp.954-961, Dec. 1987.
20. Yang W, Kelly D, Mehr I, et al., "A 3-V 340mW 14-b 75 Msample/s CMOS ADC with 85-db SFDR at Nyquist input," IEEE J. of Solid-State Circuits, Vol. 36,pp.1931-1936, Dec. 2001.
21. D. Soo, "High-Frequency Voltage Amplification and Comparison in a One-Micron NMOS Technology," Ph.D. thesis, University of California, Berkeley, 1985.
22. B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," IEEE J. Solid-State Circuits, Vol. 27, pp. 1916-1926,Dec-1992.
23. A. G.F. Dingwall,V.Zazzu, "An 8-MHz CMOS Subranging 8-Bit A/D Converter",IEEE J. of Solid-State Circuits,Vol.20,pp.1138-1143,Dec.1985.
24. Maxim, "A/D and D/A Conversion/Sampling Circuits, High-Speed Signal Processing", application Note 2085, May-2003.