Positioning of Carbon Nanotubes between Micro-electrodes for CNT-FET Fabrication

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Abstract

In this paper, the focus has been made on positioning of Single Wall Nano-tube (SWCNT) between micro-electrodes for fabrication of carbon nanotube based field effect transistor (CNTFET). The positioning is based on assembly of CNTs over the predefined self assembled monolayer of 16-Mercapto Hexadecaonoic Acid (16-MHA) ink. For nano-pattering/nano-writing of 16-MHA on gold substrate, Dip-Pen Nanolithography technique was used. Here the whole process, starting from nano-patterning of 16-MHA till CNT positioning between micro-electrodes is demonstrated successfully. The height (~2.7 nm) of nanotube in AFM image analysis of positioned carbon nanotubes, connected with micro-electrode confirms the presence of single wall CNT.

Keywords: CNT Positioning, Dip-Pen Nanolithography (DPN), CNTFET, Nano-patterning, AFM.

Introduction

One of the most significant challenges for fabrication of CNT based device is to position the nanotubes controllably and reproducibly at pre-specified locations with nanometer-scale precision. Generally two approaches have been used to control the arrangement of CNTs: First non-directed Synthesis - Nanotubes are grown first, then individually transported to the substrate and manipulated into the desired location [1]. Second: Directed synthesis involves controlled and selective growth/assembling of CNTs at pre-determined locations on the substrate [2]. Using directed synthesis high throughput yield is obtained than nondirected synthesis but directed synthesis is highly surface sensitive and CNTs orientation is determined by substrate controlled growth. In this paper patterned substrate-driven synthesis is used for CNT deposition between micro-electrodes. The CNTs were positioned on DPN generated nano-patterns of 16-MHA self-assembled monolayers. The height analysis of AFM topography image confirms the presence of SWCNT.

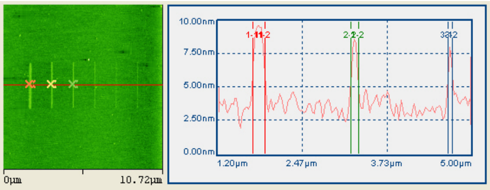
Experimental Details

N-type <111> Silicon wafers of resistivity 20-25 Ω-cm were thoroughly cleaned before actual experiments. The cleaned and dried wafers were thermally oxidized at 950^{0}C temperature to grow 250nm silicon dioxide. Photolithography followed by oxide etching using buffered oxide etchant (BOE), has been performed to make addressable substrate. These wafers were loaded in e-beam evaporation for deposition of thin film of titanium (99% pure, thickness ~4nm) and gold (99.999% pure, thickness ~20nm) to prepare the substrate for Dip-Pen nanowriting process.

For nano-writing, 16-MHA ink of concentration 4.5 mM was made in octanol solvent by sonicating the solution for 10 minutes to completely dissolve 16-MHA. AFM cantilevers were coated by above ink solution using double dipping method. These ink coated AFM tips were used for making patterns of 16-MHA using DPN (NScriptor, NanoInk). First ink calibration lines of 16-MHA were drawn to calculate diffusion coefficient, using InkCAD software [3]. Further connecting lines of 16-MHA of width 100 nm, 200 nm and 250 nm were patterned and length ranges from 10 µm to 13 µm. These SAM patterns were made on different positions between electrodes at humidity 52% and temperature 25^{0}C. CNTs do not adhere on non-polar SAM layer so remaining part of substrate was passivated with 1mM 1-octadecanethiol (1-ODT) to avoid undesired attachments. This passivated sample was dipped into SWNTs suspension of concentration 0.04 mg/ml, which was prepared in 1,2-Dichlorobenzene (DCB). The AFM images of the samples were acquired in AC mode imaging followed by image analysis in NanoRule software tool.

Results and Discussion

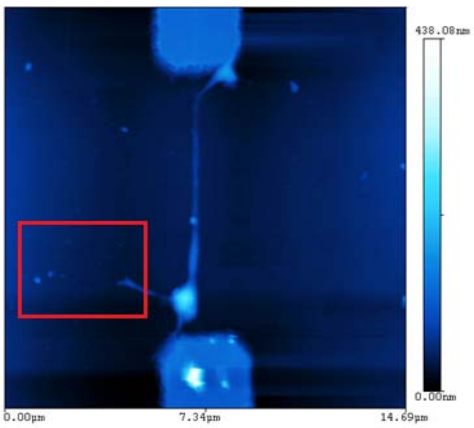
For making connecting lines of 16-MHA between micro-electrodes, first ink calibration using lines was performed with speed 0.1, 0.2, 0.4, 0.8, 1.2 and 1.6 µm/sec at relative humidity (RH) 52% and temperature 25^{0}C using DPN's InkCal module. The acquired Lateral Force Microscopy (LFM) image and its analysis are shown in Fig. 1. The calculated line diffusion coefficient from these lines is ~0.043 µm^2/sec.



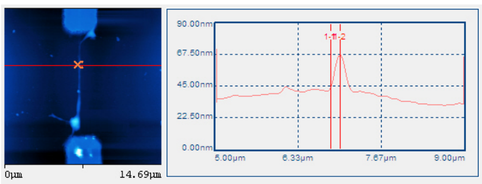
		Pair 1		Pair 2		Pair 3	
		X (μm)	Z (nm)	X (μm)	Z (nm)	X (μm)	Z (nm)
Line1	1	1.711	5.645	3.192	4.950	4.659	4.992
	2	1.894	6.335	3.310	5.462	4.725	6.509
	distance	0.183	0.690	0.118	0.513	0.066	1.517
	pt.angle	0.22 °		0.25 °		1.33 °	

Fig. 1: LFM image of ink calibration lines and width analysis of first three lines with speed 0.1, 0.2 and 0.4 µm/sec (Left to Right), at RH: 52% and Temp.: 25^{0}C.

The line, connecting micro-electrodes were written using above ink calibration. Further the substrate was passivated with 1-ODT. Passivated sample was dipped in CNT suspension for CNT positioning. Fig. 2 (a) shows the AFM topography image of positioned SWCNTs over 16-MHA nano-dimensional patterned line between microelectrodes. The upper and lower edges of positioned SWCNT show that CNTs origination from bundle (showing presence of few no. of CNTs in a bundle, as shown in Fig. 2 (a)). In Fig. 2(b) the height of pattern in AFM topography image shows attachment of SWCNTs onto written 16-MHA pattern.

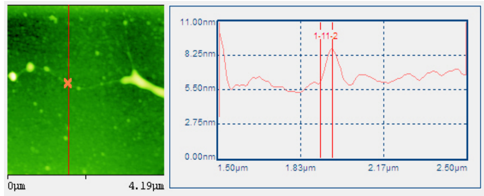


(a)



		Pair 1	
		X (μm)	Z (nm)
Line1	1	6.847	43.125
	2	7.000	67.252
	distance	0.153	24.127
	pt.angle	8.97 °	

(b)



		Pair 1	
		Y (μm)	Z (nm)
Line1	1	1.910	6.119
	2	1.958	8.821
	distance	0.049	2.702
	pt.angle	3.18 °	

(c)

Fig. 2: (a) AC mode topography image of positioned SWCNTs on 16-MHA pattern between micro-electrodes, (b) Height profile analysis of positioned SWCNTs (Height ~24 nm) and (c) Height (~2.7 nm) of SWCNTs presence in bundle of CNT, at the lower edge part (marked rectangular box) of positioned SWCNT.

Due to polar nature; strong adhere property, less angle of contact and capillary driven process of 16-MHA on dicholorobenzene solvent show that SWCNTs adhere strongly to 16-MHA SAM layer unlike SAM layer of 1-ODT. Height analysis (~ 2.7nm) of SWCNT in AFM topography images (in zoomed box as shown in Fig. 2(c)) confirms the positioning of SWCNT.

Conclusions

The attachment process of SWCNT over written 16-MHA pattern on gold substrate between micro-electrodes has been demonstrated and further confirmed from height analysis (~2.7 nm) of SWCNT in AFM topography image. This positioning process is useful for fabrication of back gate CNTFET.

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