

Neuromorphic Approach based Current Sensing Analog to Digital Converter for Biomedical Applications

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Abstract— A current sensing analog-to-digital converter (CADC) targeting biomedical applications is proposed in this paper. The proposed architecture consists of a leaky integrate and fire (LIF) neuron model inspired from neuromorphic circuits along with digital control circuits and error correction circuit to enhance INL/DNL performance. The architecture is tuned for input signal ranging from 1 μA to 64 μA with power supply of 1/1.8 V for digital and analog blocks respectively. The design is implemented in 0.18 μm CMOS 1P4M triple-well process of Tower Jazz Semiconductor's technology. Total power consumption of the circuit is 1.95 mW & 48.86 μW respectively and achieves FoM of 331.6 & 71.24 pJ/conversion-step for the cases with and without error correction for 6-bits operation.

Keywords— CADC, CMOS, LIF, FoM.

I. INTRODUCTION

Low-noise current measurement systems are gaining wider acceptance for use in biological research and biomedical instrumentation. For example, applications like rapid DNA sequencing, detection of adipocytokines, DNA sensing and measurement of ion-channel currents require bio-sensing devices such as patch-clamp, silicon nanowire and nanopore [1-3]. Such devices generate nanoampere (nA) level change in current in response to these bio-samples. Majority of bio-signals range from near DC to about 10 kHz [4].

Digitization of current signal is traditionally achieved by using low-noise and offset calibrated current-to-voltage amplifier followed by data converter *i.e.* voltage mode analog-to-digital converter (ADC). Such architectures make use of high gain OTAs as trans-impedance amplifiers [5] or high speed zero crossing detectors in pulse frequency modulation schemes [6] or switched-capacitor (SC) circuits. Charge injection errors due to switches, higher power consumption due op-amps and large silicon area due to multiple capacitors of SC circuits make them unsuitable for low-frequency biomedical applications. Similarly various direct current-to-digital converters (CDC) are reported in literature that use current controlled oscillator or sigma-delta converters with limited current range [7]. Hence, a sub-nA current sensing, wide input tunable current range CDC has wider biomedical application in both research and instrumentation.

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ADC having 64-channels and resolution of 16 bits is reported in [8] but consumes ~ 4 mW per channel. Another low power ADC having power consumption of 11 μW per channel is reported in [9], but has low input dynamic range (-100 nA to 100 nA). ADC with an input dynamic range of 10 μA to 80 μA with power consumption of 2 mW is presented in [10]. All the above reported designs have limitations either in terms of power, dynamic range or minimum input current making them less suitable for bio-medical applications.

Reported circuits based on neuromorphic approach are known to have lower power consumption and operating bandwidth of few kHz [11]. Neuromorphic designs make use of silicon neurons and synapse for their implementation and try to mimic the functionality of biological nervous system. Many neuron models have been developed depending on computational complexity and biological inspiration as shown in Fig. 1. Leaky Integrate and Fire (LIF) being mathematically simple, most frequently used, and one of the earliest silicon neurons designed, has been used in this work.

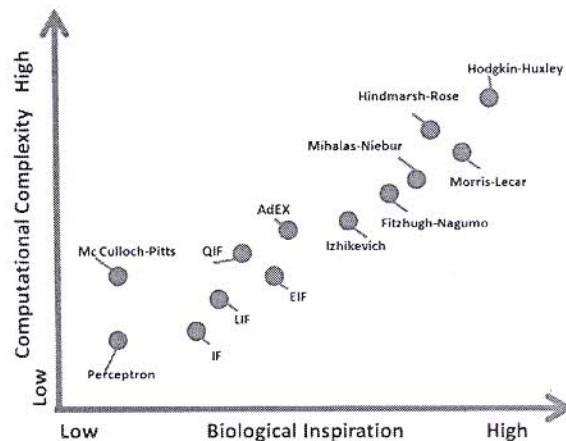


Fig. 1 Neuron computational complexity and biological inspiration [12].

The proposed CADC architecture consists of LIF, consumes less power and has on-chip error correction. The CADC makes use of current-to-frequency converter followed by frequency-to-digital conversion. Current-to-frequency

conversion is achieved with LIF neuron model. Frequency-to-digital conversion is performed by digital blocks. To reduce the power consumption and complexity of design, use of high-gain amplifiers has been avoided in CADC.

Traditionally, error correction is done in different ways depending on type of error and architecture of ADC. To illustrate, the quantization error cancelling is done using techniques like Leislie-Singh architecture, MASH architectures and non-linear effects in multi-bit converters are reduced by using dynamic element matching (DEM), trimming or digital post correction in sigma-delta ($\Sigma\Delta$) converters. Techniques like digital self-calibration, redundancy, accuracy boosting are frequently used in pipeline ADCs. There are common techniques which are used in different ADCs, such as, background calibration using histograms and correction using look up tables (LUT). LUT based correction is generic and can be applied to any type of ADC. However, the speed of error correction significantly improves in LUT technique [13].

The proposed CADC takes advantage of the low frequency bio-medical signals from bio-sensors, LIF based neuromorphic circuit using transistors in sub-threshold region and digital circuits for control and error correction. The CADC consists of LIF, adder, counter and other digital blocks to achieve 6-bits conversion accuracy. Error correction is used to reduce INL/DNL errors, thus making the design robust to errors. In the proposed CADC error correction logics are implemented using digital circuits and current comparators which generate error correction code depending on input signal and biasing currents are applied to error correction block. This error correction code is used to reduce the INL/DNL errors. Input current range tuning is also possible with altering external bias voltages, thus requiring no architectural changes.

The complete work is divided into five sections. Section II discusses the architecture of LIF in detail while section III elaborates the proposed CADC architecture. Next, in Section IV, results are given and finally, Section V concludes the work.

II. LIF ARCHITECTURE

The most frequently used neuron model in neuromorphic approach is based upon Leaky Integrate and Fire (LIF) concept. The transistor level implementation of LIF [14] has been shown in Fig. 2. Block diagram of LIF is shown in Fig. 3. Input current is integrated using integrator block after which resulting voltage is compared with the threshold voltage of the LIF set by voltage subtractor block. On exceeding the threshold voltage spike is generated by spike generation block, which also controls the frequency of spikes with the help of spike frequency control block. Therefore, input current is converted into desired spike frequency variations.

Transistors M15-M19 used in LIF perform spike frequency adaptation in neuron as shown in Fig. 4. Neurons have the ability to reduce their firing rate with spikes generated and they finally settle at low firing rate. This property is known as spike frequency adaptation. It helps in reducing the power consumption of LIF by reducing spike frequency.

In the LIF architecture shown in Fig. 2 setting V_{adap} to a finite value forces transistor M16 to allow current through it. Hence, this current generates a voltage across M17. The voltage generated across M17 is transferred and accumulated at gate of M19 whenever transistor M18 is switched on by the spike generated by LIF. Due to increasing voltage at the gate of M19, current (I_{adap}) flowing through M19 increases and results in reduction of the effective current charging C_{mem} . Due to availability of less current for charging C_{mem} there is decrease in the spike frequency at the output.

Feedback transistors M6-M7 help to charge the C_{mem} capacitor at faster rate as shown in Fig. 5. These feedback transistors help in reducing power consumption by decreasing the transition time of inverter stages.

Further, LIF is capable of generating spikes with constant frequency for wide range of input current (100 nA to 500 μ A) and can detect change in current as low as 20 nA. Lower and upper limit of input current of LIF is decided by voltages (V_{rfr} , V_{lk}) applied to LIF as shown in Fig. 6 & Fig. 7. If V_{lk} is increased in LIF then lower limit of input current shifts towards high value and therefore LIF cannot be used for currents below specified limit known as leak current of LIF. In case of upper limit, the frequency of spikes starts to saturate because of refractive period of neuron. During refractive period neuron cannot fire another spike and it has to wait for firing the next spike.

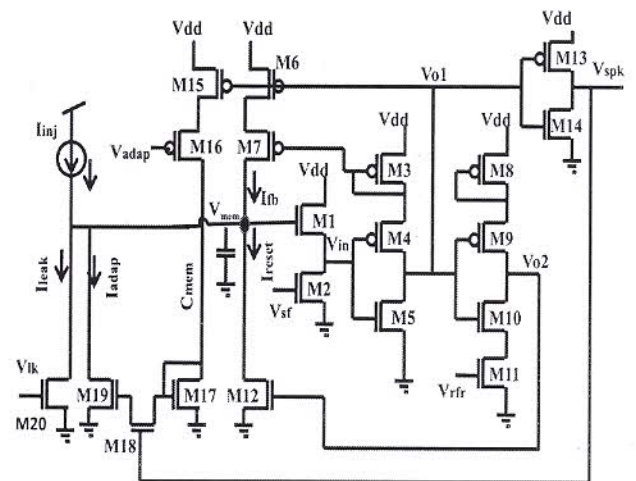


Fig. 2 Circuit of reported LIF [14].

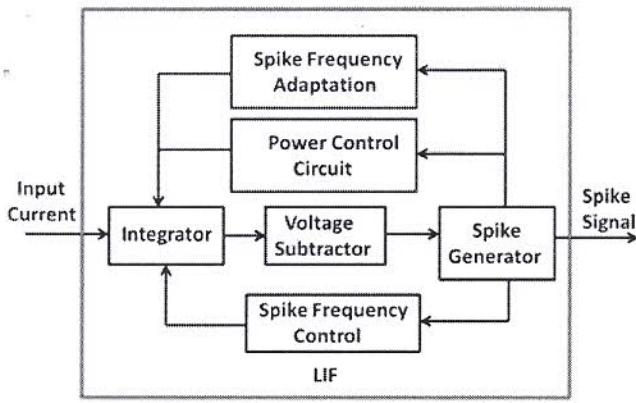


Fig. 3 Block diagram of LIF.

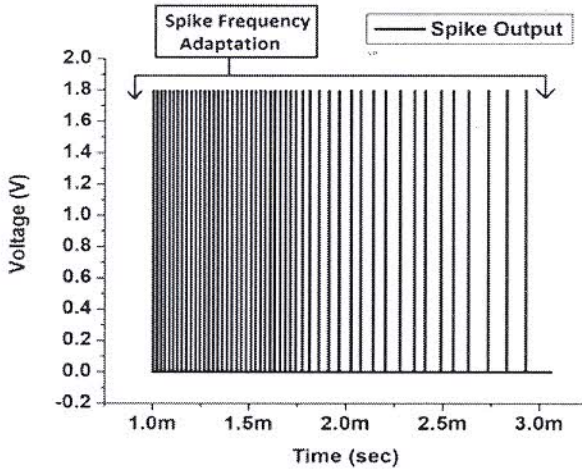


Fig. 4 Spike Frequency Adaptation in LIF.

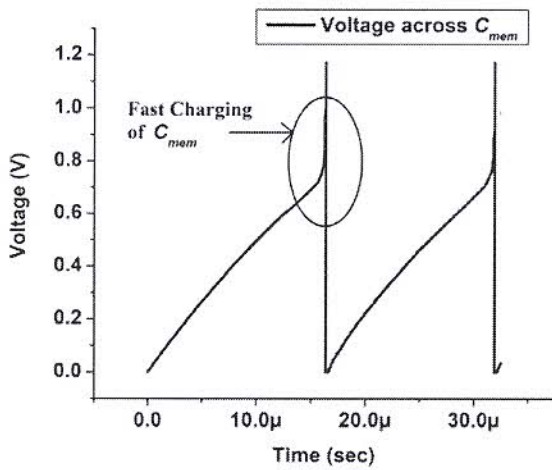


Fig. 5 Fast charging of C_{mem} in LIF.

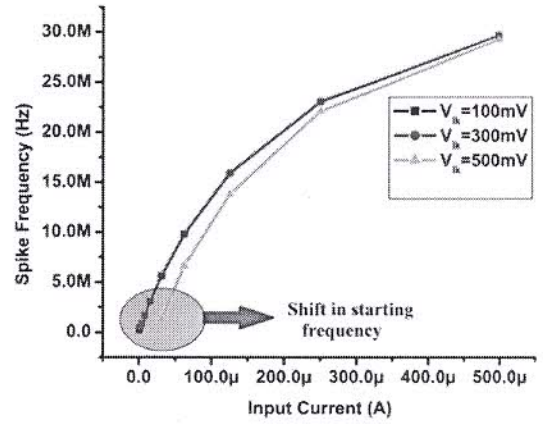


Fig. 6 Variation of Spike frequency for different V_{ik} and constant V_{fr} .

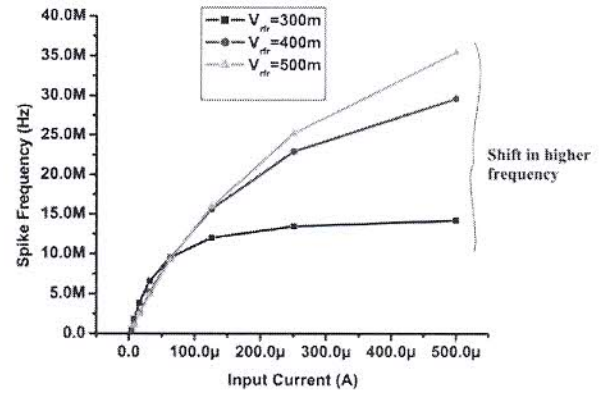


Fig. 7 Variation of Spike frequency for different V_{fr} and constant V_{ik} .

Mathematically, timing characteristics of spikes (frequency, spike width, rise time, fall time,) generated by LIF are given by (1), (2), (10) & (11).

$$F_{spike} = \frac{1}{T_W + T_{rfr} + T_c} \quad (1)$$

$$T_W = \frac{k1 * (V_{in} - V_{tn}) * C_{ginv1}}{I_{threshold}} \quad (2)$$

$$T_{rfr} = \frac{(V_{DD} - V_{tn}) * k2 * C_{gM12}}{I_{refract}} \quad (3)$$

$$T_c = \frac{C_{mem} * V_{effect}}{I_{effect}} \quad (4)$$

$$V_{effect} = \frac{V_{in}}{k} + V_{sf} \quad (5)$$

$$I_{effect} = I_{inj} - I_{leak} + I_{fb} + I_{adap} \quad (6)$$

$$I_{leak} = I_o * \left(\frac{W}{L}\right)_{M20} * \exp\left(\frac{V_{ik}}{\eta * V_{thermal}}\right) \quad (7)$$

$$I_{refract} = I_o * \left(\frac{W}{L}\right)_{M11} * \exp\left(\frac{V_{rfr}}{\eta * V_{thermal}}\right) \quad (8)$$

