Neuromorphic Approach based Current Sensing Analog to Digital Converter for Biomedical Applications

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Abstract— **A current sensing analog-to-digital converter (CADC) targeting biomedical applications is proposed in this paper. The proposed architecture consists of a leaky integrate and fire (LIF) neuron model inspired from neuromorphic circuits along with digital control circuits and error correction circuit to enhance INL/DNL performance. The architecture is tuned for input signal ranging from 1 µA to 64 µA with power supply of 1/1.8 V for digital and analog blocks respectively. The design is implemented in 0.18 µm CMOS 1P4M triple-well process of Tower Jazz Semiconductor's technology. Total power consumption of the circuit is 1. 95 mW & 48.86 µW respectively and achieves FoM of 331.6 & 71.24 pJ/conversion-step for the cases with and without error correction for 6-bits operation.**

Keywords— CADC, CMOS, LIF, FoM.

I. INTRODUCTION

Low-noise current measurement systems are gaining wider acceptance for use in biological research and biomedical instrumentation. For example, applications like rapid DNA sequencing, detection of adipocytokines, DNA sensing and measurement of ion-channel currents require bio-sensing devices such as patch-clamp, silicon nanowire and nanopore [1-3]. Such devices generate nanoampere (nA) level change in current in response to these bio-samples. Majority of bio-signals range from near DC to about 10 kHz [4].

Digitization of current signal is traditionally achieved by using low-noise and offset calibrated current-to-voltage amplifier followed by data converter *i.e.* voltage mode analog-to-digital converter (ADC). Such architectures make use of high gain OTAs as trans-impedance amplifiers [5] or high speed zero crossing detectors in pulse frequency modulation schemes [6] or switched-capacitor (SC) circuits. Charge injection errors due to switches, higher power consumption due op-amps and large silicon area due to multiple capacitors of SC circuits make them unsuitable for low-frequency biomedical applications. Similarly various direct current-to-digital converters (CDC) are reported in literature that use current controlled oscillator or sigma-delta converters with limited current range [7]. Hence, a sub-nA current sensing, wide input tunable current range CDC has wider biomedical application in both research and instrumentation.

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ADC having 64-channels and resolution of 16 bits is reported in [8] but consumes ~4 mW per channel. Another low power ADC having power consumption of 11 µW per channel is reported in [9], but has low input dynamic range (-100 nA to 100 nA). ADC with an input dynamic range of 10 µA to 80 µA with power consumption of 2 mW is presented in [10]. All the above reported designs have limitations either in terms of power, dynamic range or minimum input current making them less suitable for bio-medical applications.

Reported circuits based on neuromorphic approach are known to have lower power consumption and operating bandwidth of few kHz [11]. Neuromorphic designs make use of silicon neurons and synapse for their implementation and try to mimic the functionality of biological nervous system. Many neuron models have been developed depending on computational complexity and biological inspiration as shown in Fig. 1. Leaky Integrate and Fire (LIF) being mathematically simple, most frequently used, and one of the earliest silicon neurons designed, has been used in this work.

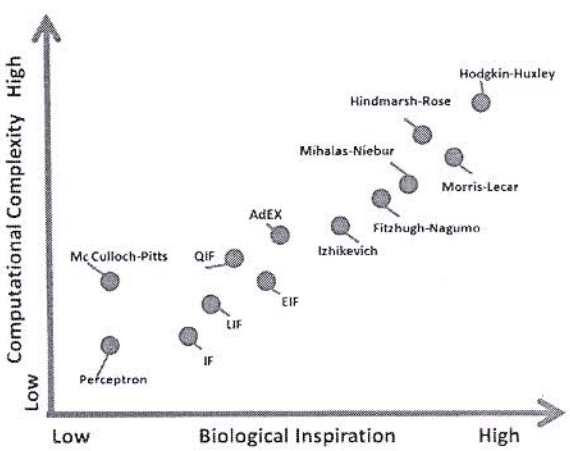

Fig. 1 Neuron computational complexity and biological inspiration [12].

The proposed CADC architecture consists of LIF, consumes less power and has on-chip error correction. The CADC makes use of current-to-frequency convertor followed by frequency-to-digital conversion. Current-to-frequency

conversion is achieved with LIF neuron model. Frequency-to-digital conversion is performed by digital blocks. To reduce the power consumption and complexity of design, use of high-gain amplifiers has been avoided in CADC.

Traditionally, error correction is done in different ways depending on type of error and architecture of ADC. To illustrate, the quantization error cancelling is done using techniques like Leislie-Singh architecture, MASH architectures and non-linear effects in multi-bit converters are reduced by using dynamic element matching (DEM), trimming or digital post correction in sigma-delta ($\sum\Delta$) converters. Techniques like digital self-calibration, redundancy, accuracy boosting are frequently used in pipeline ADCs. There are common techniques which are used in different ADCs, such as, background calibration using histograms and correction using look up tables (LUT). LUT based correction is generic and can be applied to any type of ADC. However, the speed of error correction significantly improves in LUT technique [13].

The proposed CADC takes advantage of the low frequency bio-medical signals from bio-sensors, LIF based neuromorphic circuit using transistors in sub-threshold region and digital circuits for control and error correction. The CADC consists of LIF, adder, counter and other digital blocks to achieve 6-bits conversion accuracy. Error correction is used to reduce INL/DNL errors, thus making the design robust to errors. In the proposed CADC error correction logics are implemented using digital circuits and current comparators which generate error correction code depending on input signal and biasing currents are applied to error correction block. This error correction code is used to reduce the INL/DNL errors. Input current range tuning is also possible with altering external bias voltages, thus requiring no architectural changes.

The complete work is divided into five sections. Section II discusses the architecture of LIF in detail while section III elaborates the proposed CADC architecture. Next, in Section IV, results are given and finally, Section V concludes the work.

II. LIF ARCHITECHTURE

The most frequently used neuron model in neuromorphic approach is based upon Leaky Integrate and Fire (LIF) concept. The transistor level implementation of LIF [14] has been shown in Fig. 2. Block diagram of LIF is shown in Fig. 3. Input current is integrated using integrator block after which resulting voltage is compared with the threshold voltage of the LIF set by voltage subtractor block. On exceeding the threshold voltage spike is generated by spike generation block, which also controls the frequency of spikes with the help of spike frequency control block. Therefore, input current is converted into desired spike frequency variations.

Transistors M15-M19 used in LIF perform spike frequency adaptation in neuron as shown in Fig. 4. Neurons have the ability to reduce their firing rate with spikes generated and they finally settle at low firing rate. This property is known as spike frequency adaptation. It helps in reducing the power consumption of LIF by reducing spike frequency.

In the LIF architecture shown in Fig. 2 setting V_{adap} to a finite value forces transistor M16 to allow current through it. Hence, this current generates a voltage across M17. The voltage generated across M17 is transferred and accumulated at gate of M19 whenever transistor M18 is switched on by the spike generated by LIF. Due to increasing voltage at the gate of M19, current (I_{adap}) flowing through M19 increases and results in reduction of the effective current charging C_{mem}. Due to availability of less current for charging C_{mem} there is decrease in the spike frequency at the output.

Feedback transistors M6-M7 help to charge the C_{mem} capacitor at faster rate as shown in Fig. 5. These feedback transistors help in reducing power consumption by decreasing the transition time of inverter stages.

Further, LIF is capable of generating spikes with constant frequency for wide range of input current (100 nA to 500 µA) and can detect change in current as low as 20 nA. Lower and upper limit of input current of LIF is decided by voltages (V_{rfr}, V_{lk}) applied to LIF as shown in Fig. 6 & Fig. 7. If V_{lk} is increased in LIF then lower limit of input current shifts towards high value and therefore LIF cannot be used for currents below specified limit known as leak current of LIF. In case of upper limit, the frequency of spikes starts to saturate because of refractive period of neuron. During refractive period neuron cannot fire another spike and it has to wait for firing the next spike.

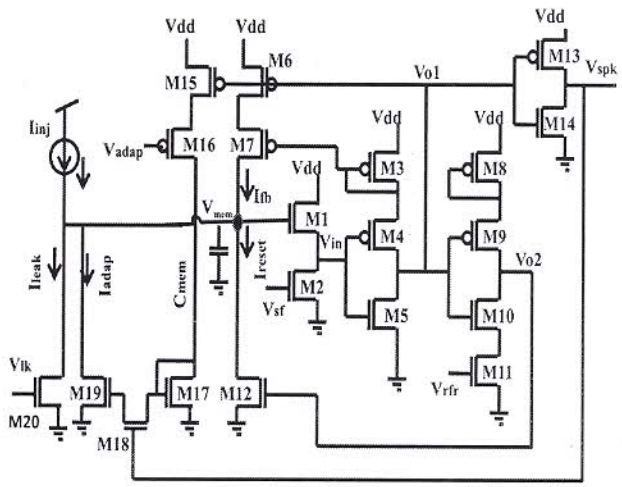

Fig. 2 Circuit of reported LIF [14].

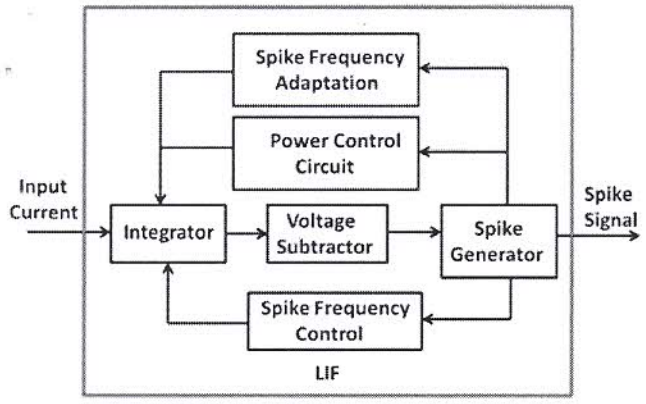

Fig. 3 Block diagram of LIF.

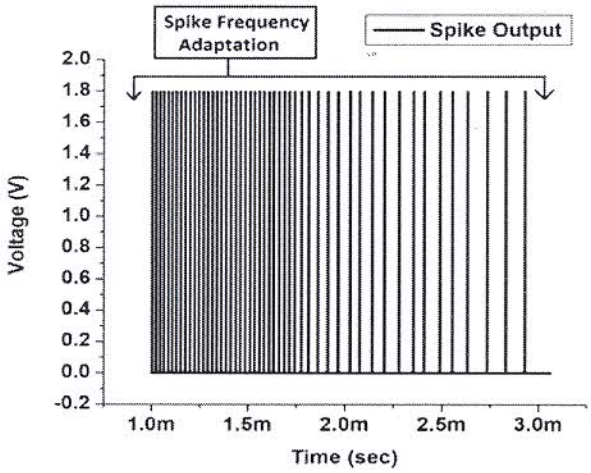

Fig. 4 Spike Frequency Adaptation in LIF.

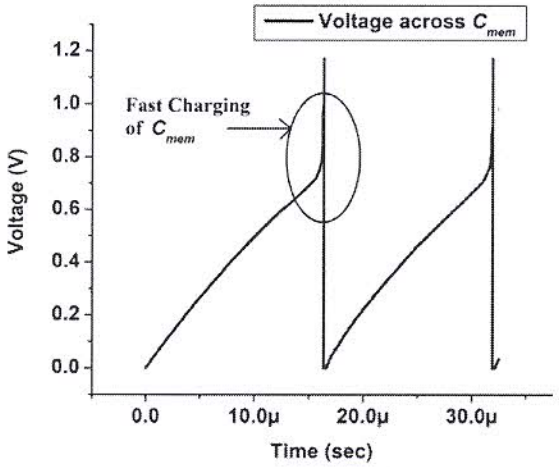

Fig. 5 Fast charging of C_{mem} in LIF.

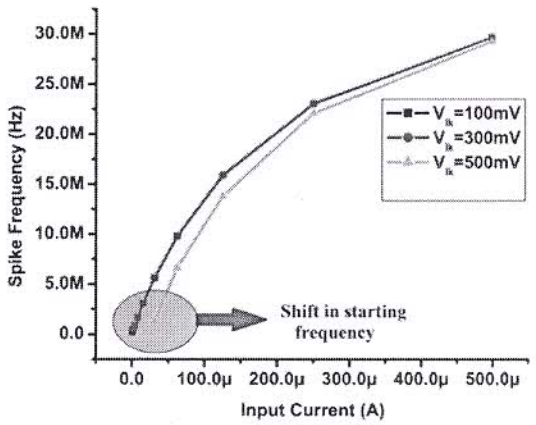

Fig. 6 Variation of Spike frequency for different V_{lk} and constant V_{rfr}

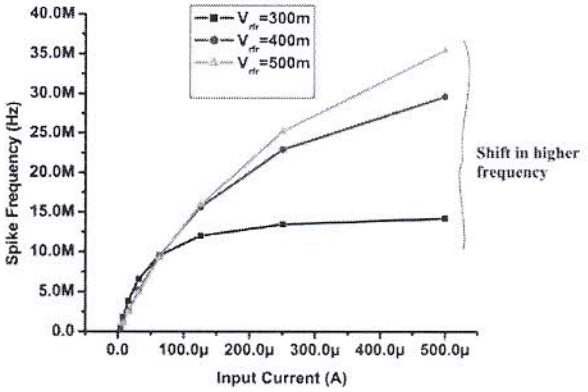

Fig. 7 Variation of Spike frequency for different V_{rfr} and constant V_{lk}

Mathematically, timing characteristics of spikes (frequency, spike width, rise time, fall time,) generated by LIF are given by (1), (2), (10) & (11).

$$F_{spike} = \frac{1}{T_W + T_{rfr} + T_c} \quad (1)$$

$$T_W = \frac{k1*(V_{in} - V_{tn})*C_{ginv1}}{I_{threshold}} \quad (2)$$

$$T_{rfr} = \frac{(V_{DD} - V_{tn})*k2*C_{gM12}}{I_{refract}} \quad (3)$$

$$T_c = \frac{C_{mem}*V_{effect}}{I_{effect}} \quad (4)$$

$$V_{effect} = \frac{V_{in}}{k} + V_{sf} \quad (5)$$

$$I_{effect} = I_{inj} - I_{leak} + I_{fb} + I_{adap} \quad (6)$$

$$I_{leak} = I_o * \left(\frac{W}{L}\right)_{M20} * exp\left(\frac{V_{lk}}{\eta * V_{thermal}}\right) \quad (7)$$

$$I_{refract} = I_o * \left(\frac{W}{L}\right)_{M11} * exp\left(\frac{V_{rfr}}{\eta * V_{thermal}}\right) \quad (8)$$

$$I_{threshold} = I_o * \left(\frac{W}{L}\right)_{M2} * exp\left(\frac{V_{sf}}{\eta * V_{thermal}}\right) \quad (9)$$

$$T_r = \left(0.86 * \left(sl * C_{load}/V_{DD} * \mu_p * C_{ox} * \left(\frac{W}{L}\right)_{M13}\right)^{1/3}\right)/sl \quad (10)$$

$$T_f = \left(0.86 * \left(sl1 * C_{load}/V_{DD} * \mu_n * C_{ox} * \left(\frac{W}{L}\right)_{M14}\right)^{1/3}\right)/sl1 \quad (11)$$

where, F_{spike} = frequency of spikes; T_W = width of spikes; T_{rfr} = refractive period of spikes (3); T_c = charging time of C_{mem} (4); C_{mem} = membrane capacitance; V_{sf} = threshold voltage of LIF (5); I_{effect} = effective current charging C_{mem} (6); I_{fb} = feedback current through M6 & M7 to reduce power consumption of neuron; I_{adap} = Adaptive current used to perform spike frequency adaptation; I_{leak} = leakage current of neuron (7); $I_{refract}$ = current through M11 (8); $I_{threshold}$ = current through M2 (9); V_{in} = logic threshold of inverter formed by transistors M3-M5; η = inverse of sub-threshold slope coefficient [14]; V_{tn} = threshold voltage of NMOS; C_{gvin1} = effective gate capacitance at node V_{in} in Fig. 2; C_{gM12} = gate capacitance of transistor M12; I_{inj} = external input to the neuron; $V_{thermal}$ = thermal Voltage; k_1,k_2 = constant value depending on process and technology; V_{sf}, V_{rfr}, V_{lk} = external voltages to control threshold voltage of neuron, refractive period of neuron and leakage current of neuron respectively; T_r = spike rise time; T_f = spike fall time; sl, $sl1$ = falling and rising slope at node V_{o1} in Fig. 2 respectively; C_{load} total capacitance at node V_{spk} in Fig. 2.

LIF achieves smaller silicon footprint (smaller capacitor footprint), in contrast to reported architectures which uses complicated and large amplifiers (continuous/switched)/ current conveyors [15].

III. Archietecture of Proposed Current Sensing Analog to Digital Converter (CADC)

Current signals are converted into digital data with the help of high-gain amplifiers, filters, and ADC. However, the proposed design makes use of silicon neurons to convert current variation into spike frequency variation using LIF. Spike output of LIF is converted into a digital output by using counter, digital control logic, buffers and clock generation circuit. The complete block diagram of CADC is shown in Fig. 8. Fig. 9 shows the chip layout with I/O pads of developed CADC using Tower Jazz 0.18 µm CMOS technology.

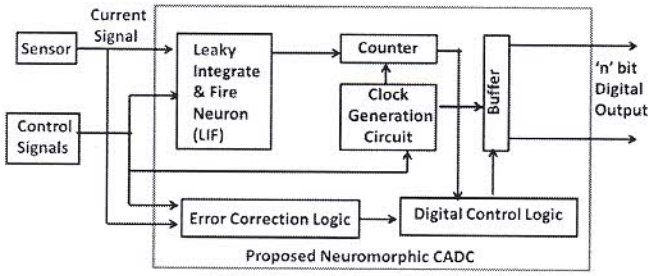

Fig. 8 Block diagram of proposed CADC.

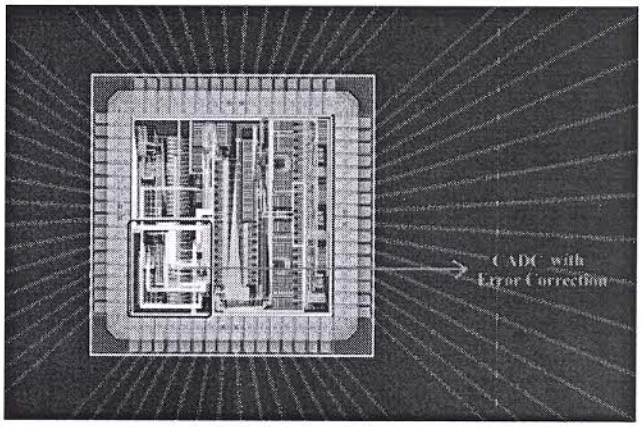

Fig. 9 Chip layout containing proposed CADC design.

Mathematically, (12), (13) and (14) give the resolution, NOB (number of bits for CADC) and output generated by the proposed CADC.

$$\text{Resolution (R)} = \frac{\text{Imax} - \text{Imin}}{2^{\text{NOB}}} \quad (12)$$

$$\text{NOB (N)} = \log_2 \frac{T_{CG}}{T_{LIF}(\text{min})} \quad (13)$$

$$\text{Digital Output} = C_o - D_o - E_r \quad (14)$$

where, I_{max} and I_{min} are the maximum and minimum input currents for which CADC is tuned.
T_{CG} = Time period of clock signal generated by clock generation circuit.
$T_{LIF}(min)$ = Time period of spikes generated by LIF for I_{max} input current.
C_o = Digital output generated by counter (bits).
D_o = Code generated by Digital control logic (bits).
E_r = Code generated by error correction block (bits).

IV. Results

Proposed CADC architecture is simulated for 6-bits operation in Cadence virtuoso environment using Tower Jazz Semiconductor's 0.18µm CMOS technology. Current to spike conversion is done using LIF. Fig. 10 shows the response of LIF for a constant input DC current of 32 µA. Variation of spike frequency for input current ranging from 0.1 µA to 500 µA is shown in Fig. 11. Variation of spike frequency for 1 µA to 64 µA current range makes LIF usable for CADC operation.

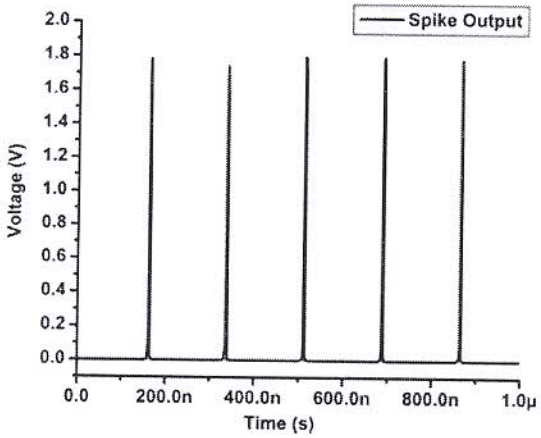

Fig. 10 Spike output of LIF.

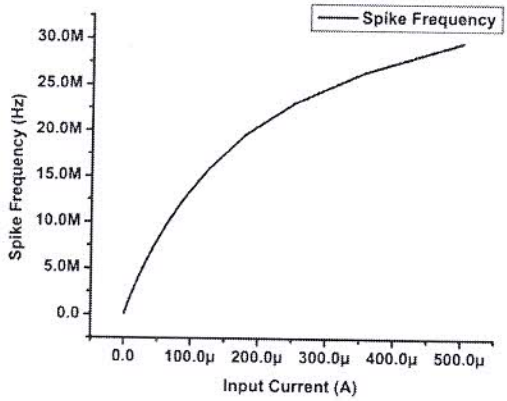

Fig. 11 Variation of frequency of spike with DC input current.

Variation of spike frequency with V_{lk} and V_{rfr} is shown in Fig. 6 and Fig. 7. V_{lk} and V_{rfr} help in estimating the lower limit and upper limit of current for which CADC can be tuned.

CADC is tuned for input current ranging from 1 μA to 64 μA with resolution of 1 μA for 6-bits operation. Decimal output value with and without error correction are shown in Fig. 12 & Fig. 13.

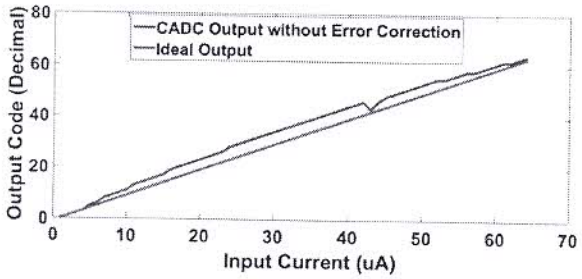

Fig. 12 Decimal output for 6-bits operation without error correction.

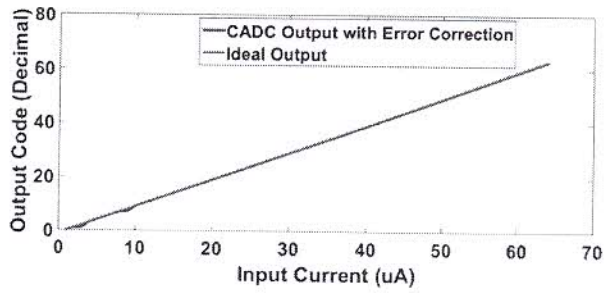

Fig. 13 Decimal output for 6-bits operation with error correction.

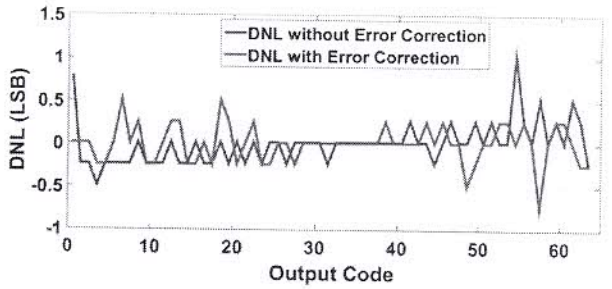

Fig. 14 DNL plots for 6-bits operation with & without error correction.

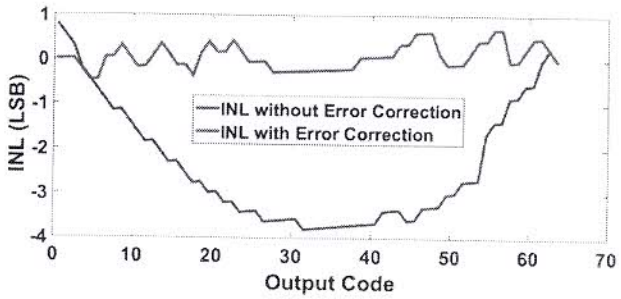

Fig. 15 INL plots for 6-bits operation with & without error correction.

Front-end of the CADC comprises of a simple integrator. Here, the absence of differential input pair in CADC relaxes the design requirements. Differential pair demands device matching, failure to which results in errors like output offset and reduction of output swing. As the proposed architecture has no high-gain amplifiers or differential pair input stage, errors due to device mismatch are absent.

Parameters of proposed CADC with and without error are listed in TABLE I. INL/DNL plots of the proposed CADC are shown in Fig. 14-15. Values of INL with and without error correction are found to be (+0.7, -0.5) & (+0.3, -3.8) respectively. DNL values with and without error correction are (+0.5, -0.5) & (+1, -0.5) respectively for 6-bits operation.

TABLE I Parameters of proposed CADC.
N/A : NOT AVAILABLE

	Parameter	Proposed CADC		[16]	
		6-bits without error correction	6-bits with error correction	6-bits	6-bits
1	Technology node	180nm	180nm	180nm	180nm
2	Capacitance used	5pF	5pF	N/A	N/A
3	Power Consumption	48.86 µW	1. 95 mW	61.3m W	121m W
4	ENOB	2.2	5.3	6	6
5	Area(mm^2)	0.044	0.212	N/A	N/A
8	Input current range	1µA-64µA	1µA-64µA	0-126µA	0-128µA
9	FoM (pJ/Conv)	71.24	331.6	20	114
10	Supply	1/1.8 V	1/1.8 V	1.8 V	1.8 V
11	INL (LSB)	0.3/ -3.8	0.7/-0.5	0.18/-0.18	0.18/-0.18
12	DNL (LSB)	0.5/-0.5	1/-0.5	0.1/-0.1	0.1/-0.1

V. CONCLUSION

CADC based on neuromorphic approach having tunable input current range, error correction, high input current range and low area is demonstrated. The proposed design is tuned for a current ranging from 1µA to 64 µA and operates with a power supply of 1/1.8 V for 6-bits. The design is capable of operating for input current range of 100 nA to 100 µA. The proposed CADC achieves FoM of 331.6 & 71.24 pJ/conv with & without error correction respectively. Further, the CADC does not require any high load driving or wide bandwidth driver stage. The achieved performance parameter values are suitable for the requirements of different biomedical applications.

ACKNOWLEDGMENT

The authors would like to acknowledge Director CSIR-CEERI, Pilani, INDIA and Dr. Chandra Shekhar (Ex. Director) CSIR-CEERI Pilani, INDIA for their support and discussions on neuromorphic approach based circuits.

REFERENCES

[1] B. Goldstein, D. Kim, J. Xu, T. K. Vanderlick and E. Culurciello, "CMOS Low Current Measurement System for Biomedical Applications," IEEE Transactions on Biomedical Circuits and Systems, vol. 6, no. 2, pp. 111-119, April 2012.

[2] G. Zang, et al., "DNA Sensing by Silicon Nanowire: Charge Layer Distance Dependence," Nano Lett. 2008, vol. 8, no. 4, pp. 1066-1070, March 2008.

[3] D. Branton, D. W. Deamer, A. Marziali, et al., "The potential and challenges of nanopore sequencing," Nature biotechnology, vol 26, no. 10, pp. 1146–1153, 2008.

[4] J. G. Webster, "Medical Instrumentation Application and Design" New York: Wiley.

[5] R. Heitz, et al., "A Low Noise Current Readout Architecture for Fluorescence Detection in Living Subjects," IEEE International Solid-State Circuits Conference, pp. 308-310, 2011.

[6] X. Wang, et al., "A High Dynamic Range CMOS Image Sensor With Inpixel Light-to-Frequency Conversion," IEEE Transactions On Electron Devices, pp. 2988-2992, 2006.

[7] M. Danesh, A. Jayaraj, S. T. Chandrasekaran and A. Sanyal, "0.43nJ, 0.48pJ/step Second-Order ΔΣ Current-to-Digital Converter for IoT Applications," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, pp. 1-5, 2019.

[8] M. Uster, T. Loeliger, W. Guggenbuhl, H. Jackel, "Integrating ADC using a single transistor as integrator and amplifier for very low (1 fA minimum) input currents," Advanced A/D and D/A Conversion Techniques and their Applications, pp. 86-89, 1999.

[9] A. Gore, S. Chakrabartty, S. Pal, E. C. Alocilja, "A Multichannel Femtoampere-Sensitivity Potentiostat Array for Biosensing Applications," IEEE Transactions on Circuits and Systems I, vol 53, no. 11, pp. 2357-2363, 2006.

[10] N. Nambiar, B. J. Blalock, M. N. Ericson, "A Current Mode Multi-Channel Wilkinson ADC," International conference on Signals and Electronic Systems, pp. 14-17, 2008.

[11] S. Furber, "Large-scale neuromorphic computing systems," Journal of Neural Engineering, 2016.

[12] S. Xiao, W. Liu, Y. Guo and Z. Yu, "Low-Cost Adaptive Exponential Integrate-and-Fire Neuron Using Stochastic Computing," IEEE Transactions on Biomedical Circuits and Systems, doi: 10.1109/TBCAS.2020.2995869.

[13] http://www.ee.oulu.fi/~timor/EC_course/chp_5.pdf

[14] G. Indiveri, "A Low-power Adaptive Integrate-and-Fire Neuron Circuit," IEEE International Symposium on Circuits and Systems, pp. 820-823, 2003.

[15] N. Singhal, M. Santosh, R. Prajesh, S. C. Bose and A. Agarwal. "Silicon Nanowire Based Platform Device for Chemical/Bio-Chemical Sensing Applications," 2018 IEEE SENSORS, 2018.

[16] S.R. Krishna et al., "Current-mode CMOS pipelined ADC," IEEE EUROCON 2009, pp.205-210.