# Design and Control of a Bi-directional *CLLC* Resonant Converter For Low voltage Energy Storage Systems

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***Abstract*— This paper presents the design of a bi-directional *CLLC* converter with an Integrated transformer for energy storage systems (ESS) applications (48 V batteries). As the distributed energy generation and storage is gaining momentum it Is required to have ESS that can regulated the power bi-directionally, presently the ESS are bulky in size, to enhance the power density and converter efficiency, an integrated transformer is introduced and simulated using 3D Finite Element Analysis (FEA). Essentially, a simple PI-based voltage/current control loop Is implemented on a 32-bit microcontroller (TMS320F28379D). Also, synchronous rectification (SR) Is implemented by controlling the turn-on and turn-off delays on rectifier sides, respectively. The design and control of the CLLC converter are verified through the experimental results. A 300 kHz, 700 W prototype Is built with the peak conversion efficiency of 96.6% while charging and 96.4% while discharging**

***Keywords—CLLC converter, Energy Storage System (ESS), Finite Element Analysis (FEA), battery charging mode (BCM), and discharging (DM)***

## I. INTRODUCTION

DC Distribution systems are gaining momentum to be the future's power system. As with the increasing demands, conventional energy sources are consumed at an exponential rate and are on the verge of extinction. The wide adoption of renewable energy sources would help to reduce the carbon footprint in the environment. Distributed generation can wave off some burden on the utility grid by storing surplus power during peak-off hours and supply the same during peak-on hours. The bi-directional converters are becoming an everlasting key component in the Distributed Generation (DG), due to its ability to condition power from a high-voltage (HV) distribution bus (Intermediate 400V DC link, or Variable 400-800V DC link, DC Electronic Load) to low-voltage (LV) distribution bus, to provide clean and stable output power and enable high reliability, effectiveness, and control of power systems. The DC distribution systems require a bi-directional AC-DC converter, which consists of a non-isolated AC-DC converter (power factor correction) and an isolated DC-DC converter (IBDC), authors in [18] developed a bi-directional AC-DC converter for DC distribution systems. Fig. 1 shows a DC-DC ESS unit converting power from an HV bus to LV batteries and vice versa.

The *CLLC* and DAB are two widely adopted topologies for DC-DC bi-directional power conversion [3][4]; the soft-switching ability is challenging to achieve in DAB converter thus, requires complex control to modulate the phase shifts

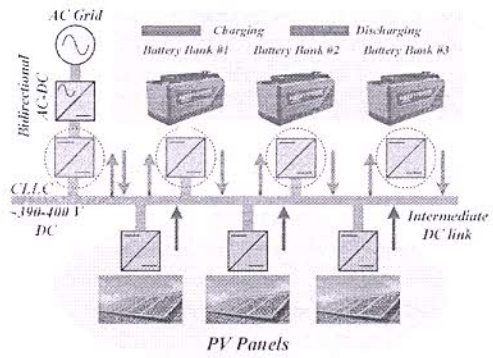


Fig. 1 *CLLC* resonant converter in a low voltage (LV) bus based Energy Storage System (ESS)

like in [16][17] the author proposes a Dual-Phase Shift (DPS) and Triple Phase Shift (TPS) modulation control. In contrast, the *CLLC* resonant converter can achieve soft-switching for full load range, while using a very simple and easy to implement control scheme of frequency modulation (FM) [2][3][7]. The implementation of bi-directional converters in [4-6][8][9] accounts for mostly (HV) outputs and no LV outputs; In the Indian scenario, the LV batteries are used for hybrid electric vehicle (HEVs), electric vehicle EVs and ESSs. In this regard, a bi-directional *CLLC* resonant converter is proposed to transfer power from an HV DC bus to LV batteries. The challenges in HV to LV power conversion is to deal with high output current in LV side which can cause severe conduction and termination loss; authors in [12][19] discusses a SR methodology; the losses due to body diode conduction can be mitigated if a synchronous rectification is used for LV sides in CM mode, respectively. A schematic of the full-bridge *CLLC* converter is shown in Fig. 2

Section II discusses the theoretical analysis of the *CLLC* converter, the FHA derived model of the *CLLC* converter,

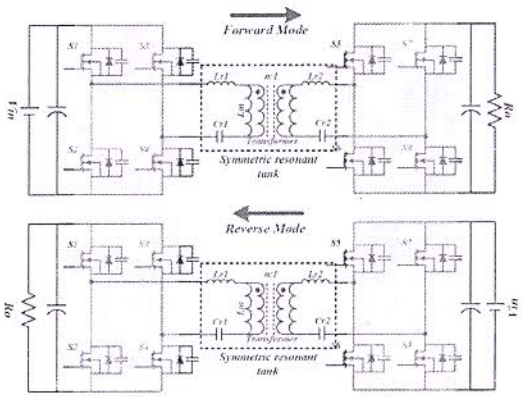


Fig. 2 Topology of *CLLC* resonant converter in charging (BCM) and discharging (DM) modes

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CM/DM mode analysis, and deduction of gain curves. Section III presents the design methodology of the *CLLC* converter for battery charging applications. Section IV presents a closed-loop control employing voltage loop control and current loop control of the *CLLC* resonant converter for charging (BCM) and discharging modes (DM). Section V presents a

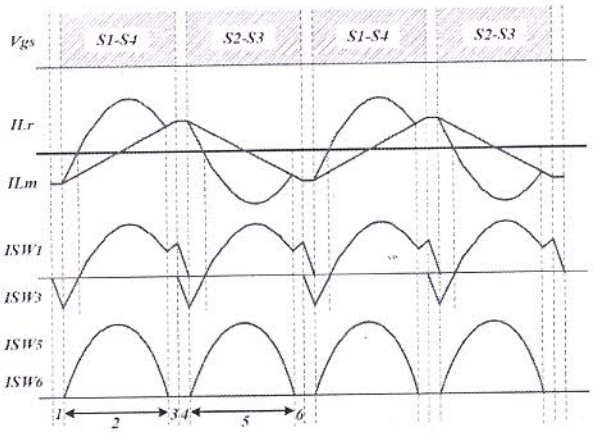



Fig. 3 Operating modes of the CLLC resonant converter at below resonance

synchronous rectification methodology for a full-bridge *CLLC* resonant converter. Ultimately, section VI concludes the design with experimental hardware results.

## II. THEORETICAL ANALYSIS

Fig. 3 illustrates the waveforms for steady stage operation of the *CLLC* resonant converter operating below the resonant frequency.

### *A. Operation of CLLC Resonant Converter*

Mode I represent a deadtime duration, during which all switches are turned off and no power is transferred to the secondary rectifying stage. The primary resonant current $I_{Lr}$, charges output capacitance of $S_3, S_4$ and discharges the output capacitance of $S_1, S_2$. After this process, the primary current passes through the anti-parallel diode of $S_1$ and $S_2$ which makes the switches operate under ZVS.

In II mode $S_1, S_2$ turns on and power is transferred through the transformer. The $I_{Lr}$ reverses its direction to positive according to $S_1, S_2$ because the input source forces the current to positive direction through $S_1, S_2$, the output voltage from the secondary is impressed on the magnetizing inductance $L_m$, then the magnetizing current $I_{Lm}$ , builds up linearly. Therefore, $L_m$ does not participate in the resonance of the primary stage.

In mode III $I_{Lr}$ equals magnetizing current, at this instant, the power transfer is stopped. Therefore, the secondary current $I_s$ becomes zero, and the output capacitor is not charged by the output current. The $I_{Lm}$ will keep rising till $S_1, S_2$ are turned off. During this mode, the $L_m$ is no longer clamped by the output voltage. Thus, $L_r, C_r$ and $L_m$ participates in resonance together, and the resonant frequency of this mode is slightly different from other modes.

Mode IV is also a deadtime duration with the switch pair $S_3, S_4$. The operation is much similar to the mode I; however, the sequence of charging and discharging switches pair is different. The $I_{Lr}$ discharges the output capacitances of $S_3, S_4$ and charges the output capacitances of $S_1, S_2$; and $S_4, S_5$ can turn on with ZVS.

In mode V $S_3, S_4$ turn on and starts transferring power to the secondary side. During this mode, the $I_{Lr}$ changes direction due to the impressed voltage but now in the opposite

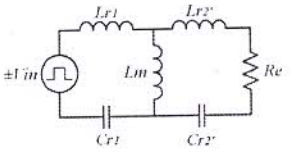



Fig. 5 FHA equivalent circuit of *CLLC* converter in DM operation

direction to that in mode II.

After the execution of Mode 5, the resonance and power transfer stops. With no power, the $I_s$ becomes zero and the anti-parallel didoes of output rectifier are softly commutated. A similar operation occurs in the reverse mode, only load, and supply voltage changes.

### *B. Gain Analysis of CLLC Resonant Converter*

#### *i. Equivalent Circuit while charging (BCM)*

The equivalent circuit of the *CLLC* converter in the forward mode is shown in Fig. 4. Assuming that '$n$' is the transformer's turns ratio. Using the FHA, equivalent load resistance $R_e$ can be expressed as follows [2][4][5][9].

$$R_e = \frac{8n^2}{\pi^2} R_o \tag{1}$$

Where, $R_o$ is the load resistance in the forward mode. All the equivalent resonant parameters referred to the primary side are as follows.

$$L'_{r2} = n^2 L_{r2}, C'_{r2} = \frac{C_{r2}}{n^2}, \tag{2}$$

The normalized frequency, quality factor, and the resonant frequency is defined as (3)

$$\omega = \frac{\omega_s}{\omega_r}, Q_f = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{R_e}, \omega_r = \frac{1}{\sqrt{L_{r1} C_{r1}}} \tag{3}$$

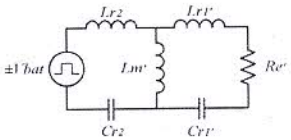



Fig. 4 FHA equivalent circuit of *CLLC* converter in BCM operation

#### *ii. Equivalent Circuit while discharging (DM)*

The Equivalent circuit of the *CLLC* converter in reverse mode is shown in Fig. 5, similar to (1) the equivalent load resistance ($R_e'$) can be calculated using FHA [2][5] and is shown in (4)

$$R_e' = \frac{8}{n^2 \pi^2} R'_o \tag{4}$$

Where, $R'_o$ is the load resistance in reverse mode. Similarly, all the resonant parameters referred to the secondary side are as follows.

$$L'_{r1} = \frac{L_{r1}}{n^2}, C_{r1} = n^2 C_{r1}, \omega_r = \frac{1}{\sqrt{L_{r2} C_{r2}}}$$

$$Q_r = \frac{\sqrt{\frac{L_{r2}}{C_{r2}}}}{R_e'}, \; L'_m = \frac{L_m}{n^2} \tag{5}$$

#### *iii. Transfer function of CLLC converter*

The general transfer function $H(s)$ can be derived by analyzing Fig. 4 and is expressed in (6)

$$H(s) = \frac{nVout}{Vin} = \frac{R_e(R_2//sL_m)}{R_2(sL_{r1}+\frac{1}{sC_{r1}}+R_2sL_m)} = \frac{Vin}{\left(\frac{1}{sC_{r1}}+sL_{r1}\right)+\left(n^2sL_{r2}+\frac{n^2}{sC_{r2}}+\frac{8n^2}{\pi^2}R_o\right)[1+\frac{1}{sL_m}(\frac{1}{sC_{r1}}+sL_{r1})]} \quad (6)$$

Where,

$$R_2 = R_e + sn^2L_{r2} + \frac{n^2}{sC_{r2}} \quad (7)$$

The gain function of *CLLC* converter in the forward mode is derived in [5], which could be expressed as (8)

$$|H(s)|_f = \frac{nV_{out}}{V_{in}} = \frac{1}{\sqrt{((\frac{1}{h}-\frac{1}{h\omega^2}+1)^2+[\frac{1}{\omega}(\frac{m}{h}+\frac{1}{hg}+\frac{1}{g}+1)Q_f-\omega(\frac{m}{h}+m+1)Q_f-\frac{Q_f}{hg\omega^3}]^2)}} \quad (8)$$

Where,

$$h = \frac{L_m}{L_{r1}}, m = \frac{n^2L_{r2}}{L_{r1}}, g = \frac{C_{r2}}{n^2C_{r1}}$$

Similarly, the gain function for reverse mode can be expressed as in (9)

$$|H(s)|_r = \frac{1}{\sqrt{((\frac{1}{p}-\frac{1}{p\omega^2}+1)^2+[\frac{1}{\omega}(\frac{r}{p}+\frac{1}{pq}+\frac{1}{q}+1)Q_r-\omega(\frac{r}{p}+r+1)Q_r-\frac{Q_r}{pq\omega^3}]^2)}} \quad (9)$$

Where,

$$p = \frac{L_m}{n^2L_{r2}}, r = \frac{L_{r1}}{n^2L_{r2}}, q = \frac{n^2C_{r1}}{C_{r2}}$$

*iv. Primary side zero voltage switching (ZVS) consideration*

ZVS is achieved whenever the converter is operating in the inductive region or the slope of gain curves is negative. As mentioned in [2], to achieve ZVS on the primary side of the converter, the magnetizing current must be sufficient to discharge the output capacitances of the primary side MOSFETs (in this case GaN MOSFETs) within deadtime. Thus, the $L_m$ should be limited to a maximum value [2], given by (10)

$$L_m \leq \frac{T_{dead}}{16C_{oss}f_{smax}} \quad (10)$$

Where, $T_{dead}$ is the dead time, $C_{oss}$ is the MOSFET junction capacitance, and $f_{smax}$ is the maximum switching frequency.

## III. Design Methodology

### A. Considerations of Design Parameters

In this paper, the converter is designed with 700 W of output power rating. The input voltage range is chosen as 360-400 V DC and the output voltage range is 45-54 V DC. The resonant frequency $F_r$ is selected 350 $kHz$ for charging (BCM) and 300 $kHz$ for discharging (DM) modes considering the trade-offs between EMI, power density, and efficiency. Reducing the resonant frequency can help in the reduction of core and copper losses in the transformer but, may cause severe EMI issues [14]. The resonant converters have advantages of operating at a wide input/output voltage range; the converter aims at charging an ESS battery pack of voltage range 42-54 V (13 Cell Li-Ion Pack). The turns ratio for the *CLLC* converter can be calculated as:

$$n = \frac{V_{in}}{V_{out}} = \frac{400}{50} = 8 \quad (11)$$

To maximize the converter's efficiency is it recommended to operate it at resonant frequency [10]; this reduces circulating power loss and minimizes the current distortion. It is desired to have monotonic gain curves to implement linear control (PI); if not, then the non-linear control scheme has to opt which increases the control complexity and is not preferred for this application. Smaller $Q$ factor can provide monotonic gain curves, while a large $Q$ factor facilitates narrow frequency range. The nominal output resistance in CM mode is 5Ω with 50 V output voltage and in DM mode is 330Ω with 400 V output voltage. Based on the turn ratio, the gain range is designed to be 0.9-1.08 in BCM mode and 0.92-1.1 in DM mode, respectively. This gain arrangement satisfies the wide output range requirement of the converter. The resonant elements can be calculated via equations (1-3) for charging mode and (4-5) for discharging modes; resonant capacitor and leakage inductance can be calculated as:

$$C_{r1} = \frac{1}{2\pi f_r Q_f R_e} \quad (12)$$

$$L_{r1} = \frac{1}{2\pi {f_r}^2 C_{r1}} \quad (13)$$

To reduce the size and weight of the converter, leakage inductance of the transformer is utilized as resonant inductors. Table. I enlist the designed parameters for the *CLLC* converter. Fig. 6 shows the MATLAB plotted gain curves for BCM and DM modes, respectively.

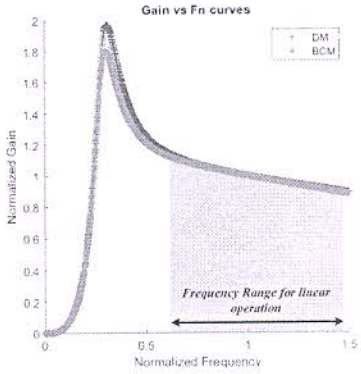



Fig. 6 Gain curves obtained via MATLAB plots for BCM and DM modes

TABLE I. KEY DESIGN PARAMETERS OF *CLLC* RESONANT CONVERTER

| Parameters | Forward | Reverse |
|---|---|---|
| Resonant frequency $F_r$ $(kHz)$ | 350 | 300 |
| Gain range | 0.9-1.08 | 0.98-1.06 |
| Input Voltage Range (V) | 340-380 | 40-60 |
| Output voltage range (V) | 40-60 | 360-400 |
| Primary resonant capacitor $C_{r1}$ | $11nF$ | |
| Secondary resonant capacitor $C_{r2}$ | $1\mu F$ | |
| Primary resonant inductance $L_{r1}$ | $17\mu H$ | |
| Secondary resonant inductance $L_{r2}$ | $260nH$ | |
| Magnetizing inductance $L_m$ | $120\mu H$ | |

### B. Design of Integrated PlanarTransformer

To achieve high conversion efficiency, it is desired to mitigate core and winding losses; additionally, to reduce the weight and volume of the converter, an integrated transformer is adopted in this design. The windings are made of PCB stacks each for the primary and secondary sides. To utilize leakage inductances as resonant inductors, both primary and secondary windings are separated by a winding gap $l_b$; by varying this gap, the leakage inductance of both primary and secondary sides can be adjusted to the required value. An air gap is provided between core legs to avoid

saturation. Considering the power ratings and air gap margins; ELP38/8/25 core and 3F4 material from Ferroxcube is selected. As the number of turns increases, flux density in the core material decreases; thus, the number of turns in primary and secondary sides are kept as 16 and 2, respectively. Primary winding comprises of 4 PCB stacks of 4 turns each in series, and secondary winding comprises of 4 PCB stacks of 2 turns each in parallel, shows in Fig, 7. PCB stacks are used to mitigate the skin and proximity effect caused by high-frequency AC in windings. Table. II summarizes the parameters of an integrated transformer.

TABLE. II KEY PARAMETERS OF INTEGRATED PLANAR TRANSFORMER

| Parameters | Value |
|---|---|
| Turns ratio $Np$: $Ns$ | 8:1 |
| Core Size | ELP 38/8/25 -2 |
| Core material | 3F4 |
| Leakage air gap (mm) | 0.9 |
| Core air gap (mm) | 0.7 |

FEA is performed to obtain magnetic flux density. Fig. 8 shows the FEA simulated results of the designed integrated planar transformer. The maximum flux density is near the air gap proximity region (0.288T), which is still below the saturation flux density (0.4T) of the core material. Compared to the Litz wire winding based magnetic structures, PCB winding based magnetics are more sensitive to the high-frequency AC winding loss [15]. The skin effect can have a significant effect on the winding loss at higher frequencies

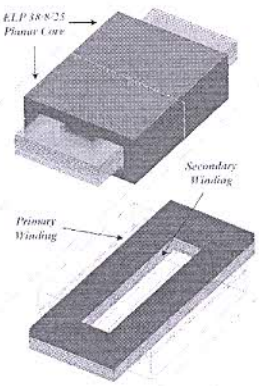



Fig. 7 Construction of planar integrated transformer

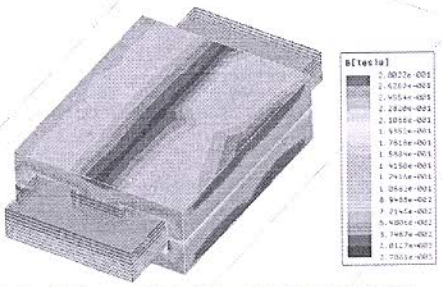



Fig. 8 FEA simulation results for Magnetic flux density (B)

due to increased proximity effect between each turn, making AC resistance significantly high. Considering the 1D model as per [20]

$$\begin{cases} F_R = \dfrac{R_{AC}}{R_{DC}} = M' + \dfrac{(m^2-1)D'}{3} \\ M = \delta h \coth \delta h \\ D = 2\delta h \tanh \delta h/2 \end{cases} \quad (14)$$

$$\begin{cases} \delta = \sqrt{\dfrac{j\omega\mu_o\eta}{\rho}} \\ \eta = \dfrac{aN_l}{b} \end{cases} \quad (15)$$

Where, $F_R$ is the ratio of AC winding resistance to the DC winding resistance, $M'$, $D'$ are the real parts of $M$ and $D$, $h$ is the height of the conductor (which in this case is the thickness of copper in PCB), $\mu_o$ is the permeability of free space, $a$ is the width of the conductor, $Nl$ is the number of turns per layer, and $b$ is the window width. Using the above equations, $F_R$ can be calculated as 3.579. Thus, the AC resistance of windings can be calculated as:

$$R_{AC} = F_R R_{DC} \quad (16)$$

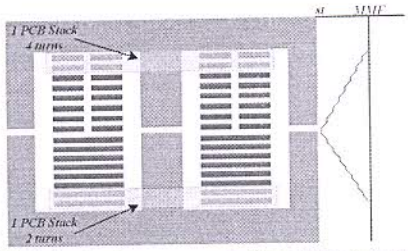



Fig. 9 (a) MMF distribution among windings of the transformer (b) developed integrated planar transformer

Fig. 9 shows the MMF distribution, winding arrangement, and developed an integrated planar transformer. Though the MMF across each stack is high compared to the interleaved structures [15], this winding arrangement fulfills the requirement of a resonant inductor.

## IV. CLOSED-LOOP CONTROL OF THE *CLLC* CONVERTER

Frequency modulation (FM) is the conventional control for any resonant converter. FM is widely used for LLC and *CLLC* resonant converters. Thus, to keep the control system simple and easy to implement, FM is adopted. Voltage loop control and current loop control are implemented as a part of constant current (CC) and constant voltage (CV) charging and discharging. A PI controller is used to implement the voltage loop control and current loop control, respectively; the transfer function of the PI controller is given as (17)

$$C(s) = K_p + \frac{K_i}{s} \quad (17)$$

Increasing $K_p$ may result in faster dynamic response, but jeopardizes the phase margin and thus stability of the control loop. Equation (6) can be used to derive the expression for output voltage $V_o(s)$; a partial derivative with respect to the variable $s$ would give a plant transfer function $T_P(s)$ [12] which can be derived as (18)

$$T_P(s) = \frac{\partial V_o(s)}{\partial s} = \frac{8n^2R_oV_{in}}{\pi^2} \frac{\frac{1}{s^2C_{r1}} - L_{r1} + \frac{n^2L_{r2} - \frac{n^2}{s^2C_{r2}}}{s^3L_mC_{r1}}}{\left\{\left(\frac{1}{sC_{r1}} + sL_{r1}\right) + \left(n^2sL_{r2} + \frac{n^2}{sC_{r2}} + \frac{8n^2}{\pi^2}R_o\right)\left[1 + \frac{1}{sL_m}\left(\frac{1}{sC_{r1}} + sL_{r1}\right)\right]\right\}^2} \quad (18)$$

Fig. 10 (a) shows the open-loop bode plot of plant transfer function the *CLLC* resonant converter. Multiplying the plant transfer function by PI compensator's transfer function gives the loop gain of the control system. The closed-loop transfer function of the control system $G(s)$ can be derived as

$$G(s) = \frac{C(s)T_P(s)}{1+C(s)T_P(s)} = \frac{K_p+\frac{K_i}{s}}{K_p+\frac{K_i}{s}+\frac{\pi^2\left\{\left(\frac{1}{sC_{r1}}+sL_{r1}\right)+\left(n^2sL_{r2}+\frac{n^2}{sC_{r2}}+\frac{8n^2}{\pi^2}R_o\right)\left[1+\frac{1}{sL_m}\left(\frac{1}{sC_{r1}}+sL_{r1}\right)\right]\right\}}{8n^2R_oV_{in}\left(\frac{1}{s^2C_{r1}}-L_{r1}+\frac{n^2L_{r2}-\frac{n^2}{s^2C_{r2}}}{s^3L_mC_{r1}}\right)}}^2 \quad (19)$$

Where, $C(s)$ is the transfer function of the PI controller, Fig.

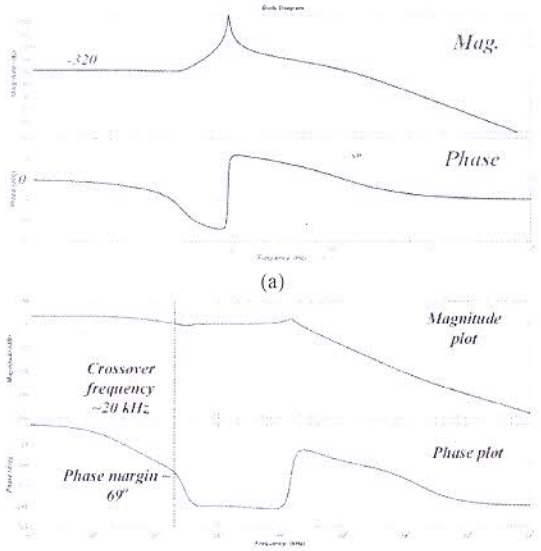



Fig. 10 (a) uncompensated bode plot of plant transfer function for *CLLC* converter (b) compensated bode plot of closed loop transfer function for the *CLLC* converter

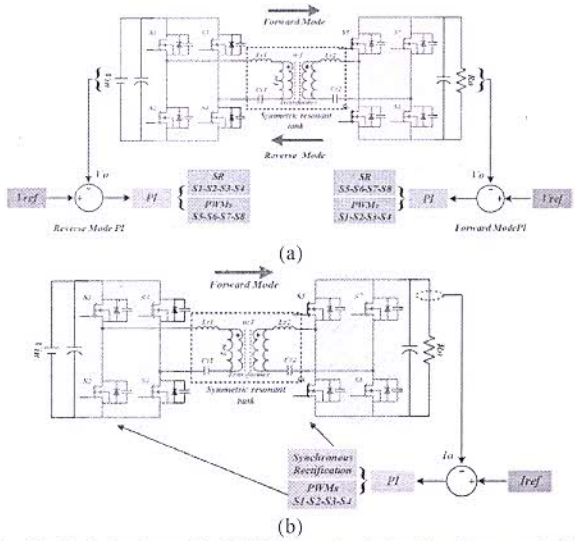



Fig. 11 Control scheme for *CLLC* converter (a) voltage loop control in BCM and DM mode (b) current loop control in BCM mode

10 (b) validates the stability of the control loop; where the phase margin is around $69^o$ and cross-over frequency is chosen at 20 kHz, respectively. The PI controller is implemented in a 32-bit digital microcontroller (TMS320F28379D). Fig. 11 (a) shows the voltage loop control and current loop control of the *CLLC* converter while charging and discharging. Fig. 11 (b) shows the current loop control of the *CLLC* converter while charging. Only the voltage loop control is considered while discharging; as the load may not be a stiff voltage source thus, needed to be maintained.

## V. Synchronous Rectification

Due to the resonant tank characteristics, an inherent phase shift exists between the primary side gate pulses and secondary side resonant current. This phase shift can be denoted by $\delta$ and it depends on the resonant tank elements and operating frequency [9][10]. This phase angle can be measured experimentally by keeping SR turned off and conduction occurred via body diodes of the MOSFETs. The switches on the secondary side must be synchronized with the polarity of the secondary-side resonant current. If the turn-on timing of SRs is not aligned properly; there would be circulating current in the secondary resonant tank which would further increase conduction losses. Fig. 12 (a) shows the body diode conduction path (no circulation loss) (b) shows the conduction path of the circulating current if SRs

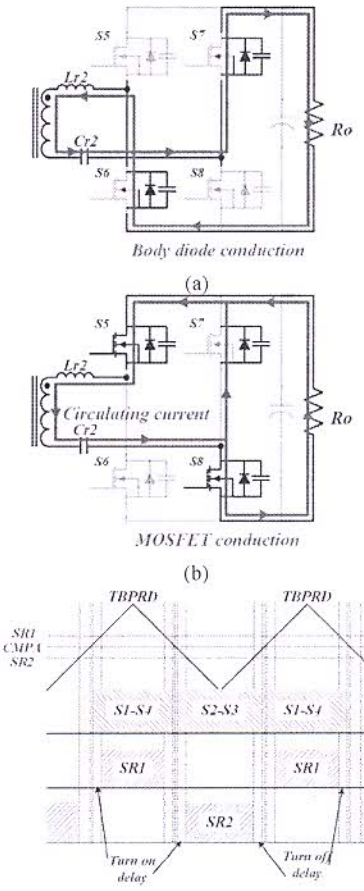
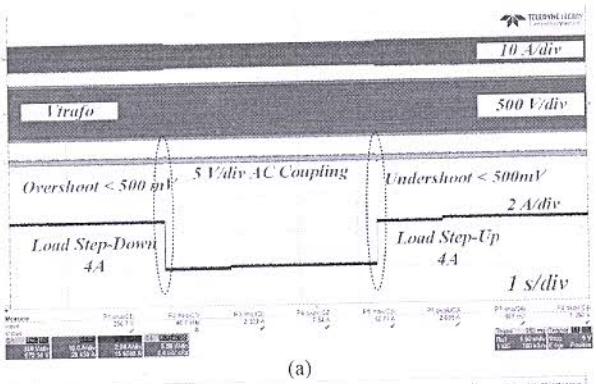



Fig. 12 (a) body diode conduction and proper SR operation (b) mismatched SR signals causing circulating current in secondary winding (c) Microcontroller based SR control scheme

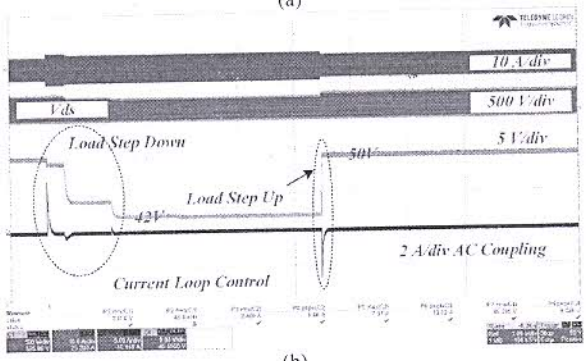
are not engaged properly as per the polarity of the secondary-side resonant current, and (c) shows the SR scheme's implementation in microcontroller, both SR signals are complement to each other and involve different turn-on and off delays. This circulation causes additional conduction losses in the secondary MOSFETs (SRs in CM) and transformer windings. As a consequence, this degrades the conversion efficiency. Authors in [19] proposed a method to execute SR operation for high-frequency applications.

## VI. Experimental Hardware Results

An Experimental prototype with GaN MOSFETs of the bi-directional converter is built and shown in Fig. 13. The rated

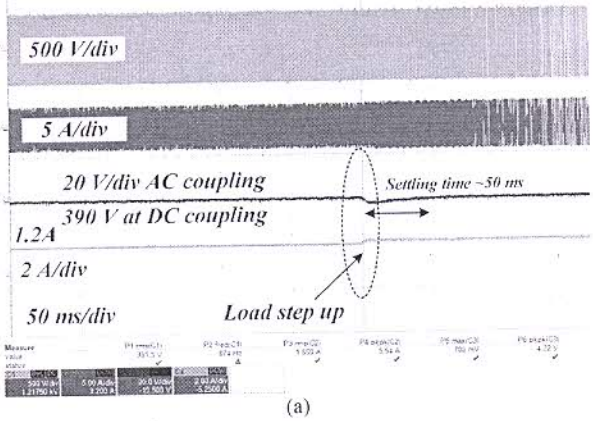



(a)

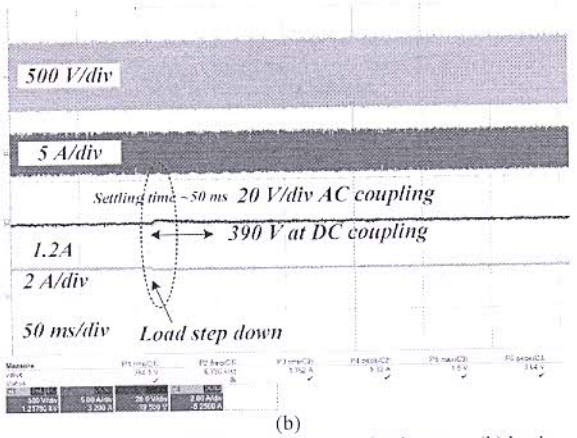



(b)

Fig. 15 closed loop load transients in *CLLC* converter (a) voltage loop control 500-300W and 300-500W (b) current loop control 450-380W and 380-450W




(a)




(b)

Fig. 16 Load transients during DM mode (a) load step-up (b) load step-down

charge and discharge power is 700 W with 350 kHz of switching frequency while charging and 300 kHz while discharging. Fig. 14 (a) shows the steady-state waveforms of the *CLLC* converter in charging mode and (b) in discharging mode, and (c) thermal profile, respectively. To validate the

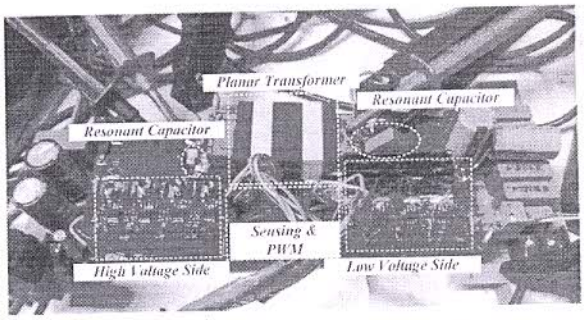
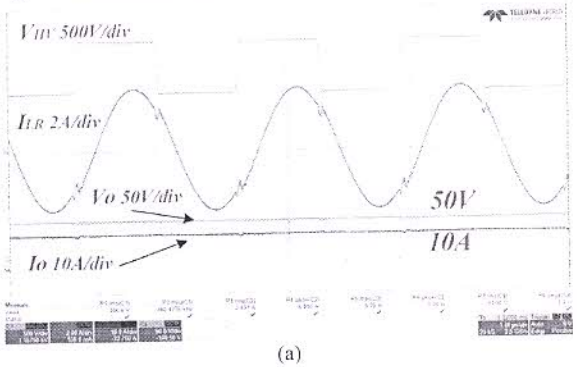
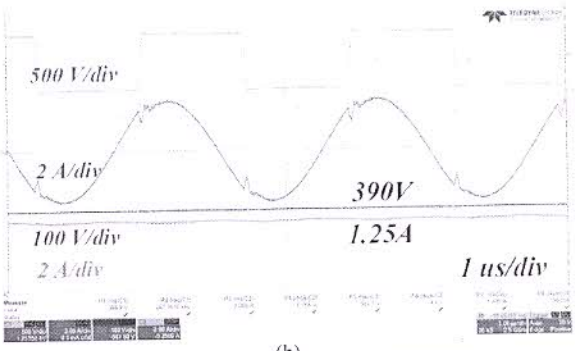


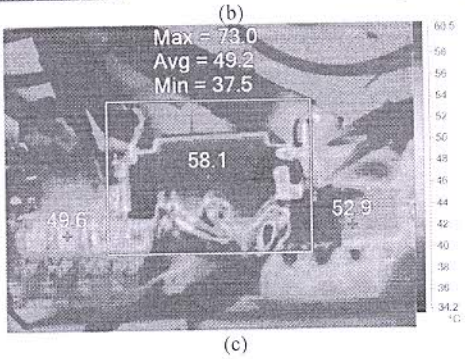

Fig. 13 Hardware prototype of *CLLC* resonant converter




(a)




(b)




(c)

Fig. 14 Steady state hardware results for *CLLC* resonant converter in (a) battery charging mode (BCM) (b) discharging mode (DM) and (c) thermal profile of the converter operating at steady state

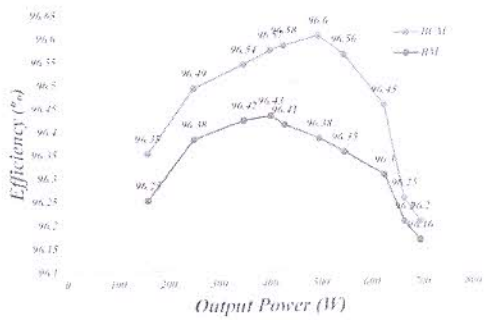



Fig. 17 Conversion efficiency of *CLLC* resonant converter

control schemes, load transient tests are performed. Fig. 15 (a) shows the closed-loop voltage transient from 500-300 W and 300-500 W; (b) closed-loop current transient from 450-380 W and 380-450W in CM mode, respectively. Fig. 16 (a, b) shows the voltage loop transient for DM mode.

## CONCLUSION

In this paper, the design for the *CLLC* converter for LV output with SR is discussed. As a part of the design, resonant tank elements are optimized for improved efficiency and power density. The closed-loop control is implemented as current loop control and voltage loop control for CC/CV in BCM, and the voltage loop control is implemented for DM operation. The experimental results are presented to verify the effectiveness of the proposed control methods and SRs. The peak efficiencies reach 96.6% in BCM mode and 96.4% in DM mode, respectively.

## ACKNOWLEDGMENT

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