Design of Bi-directional *CLLC* Resonant Converter with Planar Transformer and Synchronous Rectification for Energy Storage Systems

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***Abstract*— This paper presents the design of a bi-directional *CLLC* resonant converter for low-voltage energy storage systems (48V) applications. Usually the power desnity for such converters are low due to low switching frequency operation. Thus for first step the swithcing frequency is kept ~300-350 kHz to reduce the size of passives components, which facilitates the usage of planar transformers to enhance power density. Generally the current on LV side is high and to mitigate this a synchronous rectification (SR) scheme is devised. FEA analysis is performed to verify the design of planar transformer for peak flux density, core and copper losses. The SRs and control loop (PI) is implemented via a 32-bit Microcontroller (TMS320F28379D) for CC/CV control in charging mode (CM) and Dishcharging Mode (DM) respectively. This proof of concept prototype is verfified through a 700W hardware prototype using GaN MOSFETs at high voltage and Silicon MOSFETs at low voltage side; achieving an efficiency of 96.6% in CM and 96.4% In DM.**

Keywords—CLLC converter, Energy Storage System (ESS), Finite Element Analysis (FEA), Charging Mode (CM), Discharging Mode (DM), and Gallium Nitride (GaN)

I. INTRODUCTION

DESs are emerging as an alternative to conventional energy sources to some extent; comprising of renewable sources of energy like photovoltaic (PV) and wind energy systems (WECS). DES can effectively support the energy requirements during peak load hours and can supply surplus energy to the utility grid during peak off hours. In this regard, a bi-directional resonant *CLLC* converter is proposed for battery charging mode (BCM) and reverse mode (RM) employing integrated planar transformer and synchronous rectification. *CLLC* and DAB are two widely adopted topologies for bi-directional power conversion [1]; for DAB converter, soft-switching is a challenge at light load; thus require complex control like in [3] to compensate for light-load efficiency. *CLLC* converter employs a frequency modulation (FM) scheme to control the dynamics of the resonant tank and regulate output power. The most widely adopted bi-directional power converters only account for high voltage (HV) outputs [5][6].

The DC distribution systems require a bi-directional AC-DC converter, which consists of a non-isolated AC-DC converter (power factor correction) and an isolated DC-DC converter (IBDC), authors in [18] developed a bi-directional AC-DC converter for DC distribution systems. Fig. 1 shows an ESS converting power from a HV bus to LV batteries bi-directionally.

The *CLLC* and DAB are two widely adopted topologies for DC-DC bi-directional power conversion [4]; the soft-switching ability is challenging and is subject to load conditions in DAB converter thus, requires complex control to modulate the phase shifts like in [19][20].In constrast, the *CLLC* resonant converter can achieve soft-switching for full load range, despite using a very simple and easy to implement control scheme of frequency modulation (FM) [2][3][7].

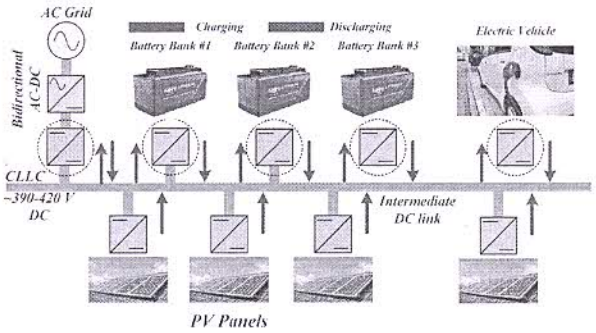

Fig. 1 *CLLC* resonant converter in a low voltage (LV) bus based Energy Storage System (ESS)

Apparantly most of the isolated bi-directional converters in [4-6][8-9] accounts for mostly high-voltage (HV) outputs and none LV outputs. In Indian scenario, the LV batteries are used for hybrid electric vehicle (HEVs), electric vehicle EVs and ESSs. In this regards, a bi-directional *CLLC* resonant converter is proposed to charge/Discharge LV batteries. The challenges in HV to LV power conversion is to deal with high output current in LV side which can cause severe conduction and termination loss. Thus, a synchronous rectification scheme is devised to enhance conversion efficiency. Section II discusses the theoretical analysis of the *CLLC* converter, the FHA derived model of *CLLC* converter, CM/DM mode analysis, and derivation of gain curves. Section III presents the design methodology of a *CLLC* resonant converter for battery charging application. Section IV presents the design of a planar transformer using analytical methods and FEA

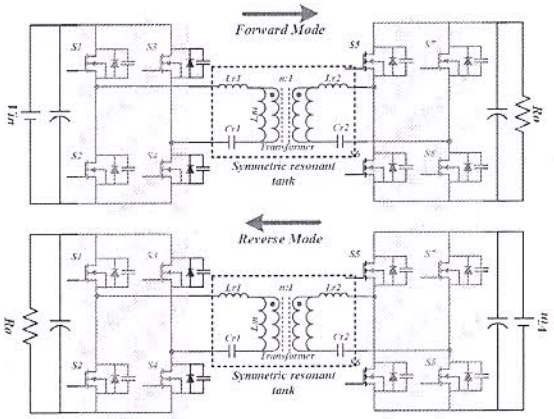

Fig. 2 Topology of *CLLC* resonant converter in charging (CM) and discharging (DM) modes

simulations. Section V presents a synchronous rectification methodology for full bridge *CLLC* resonant converter. Section VI discusses the control system for CC/CV charging of LV batteries. Ultimatley, the section VII concludes the design of a *CLLC* resonant converter by depicting simulation and hardware steady state/dynamic results.

II. THEORETICAL ANALYSIS OF *CLLC* RESONANT CONVERTER

Fig. 3 illustrates the waveforms for steady stage operation of the *CLLC* resonant converter operating below the resonant frequency.

A. Operation Modes of a CLLC Resonant Converter

Mode I represent a deadtime duration, during which all switches are turned off and no power is transferred to the secondary rectifying stage. The primary resonant current I_{Lr}, charges output capacitance of S_3, S_4 and discharges the output capacitance of S_1, S_2. After this process, the primary current passes through the anti-parallel diode of S_1 and S_2 which makes the switches operate under ZVS.

In II mode S_1, S_2 turns on and power is transferred through the transformer. The I_{Lr} reverses its direction to positive according to S_1, S_2 because the input source forces the current to positive direction through S_1, S_2, the output voltage from the secondary is impressed on the magnetizing inductance L_m, then the magnetizing current I_{Lm} , builds up linearly. Therefore, L_m does not participate in the resonance of the primary stage.

In mode III I_{Lr} equals magnetizing current, at this instant, the power transfer is stopped. Therefore, the secondary current I_s becomes zero, and the output capacitor is not charged by the output current. The I_{Lm} will keep rising till S_1, S_2 are turned off. During this mode, the L_m is no longer clamped by the output voltage. Thus, L_r, C_r and L_m participates in resonance together, and the resonant frequency of this mode is slightly different from other modes.

Mode IV is also a deadtime duration with the switch pair S_3, S_4. The operation is much similar to the mode I; however, the sequence of charging and discharging switches pair is different. The I_{Lr} discharges the output capacitances of S_3, S_4 and charges the output capacitances of S_1, S_2; and S_4, S_5 can turn on with ZVS.

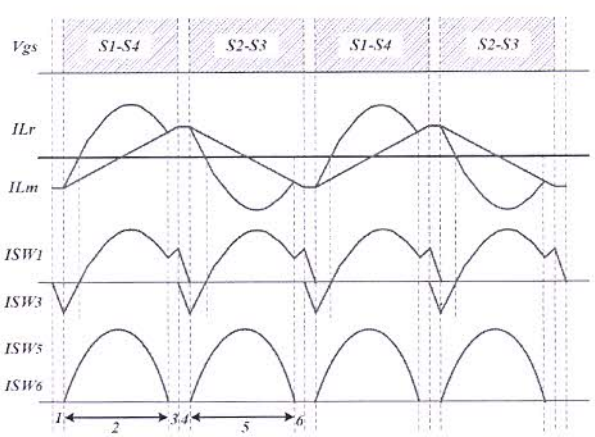

Fig. 3 Operating modes of the *CLLC* resonant converter operating below resonance

In mode V S_3, S_4 turn on and starts transferring power to the secondary side. During this mode, the I_{Lr} changes direction due to the impressed voltage but now in the opposite direction to that in mode II.

After the execution of Mode 5, the resonance and power transfer stops. With no power, the I_s becomes zero and the anti-parallel didoes of output rectifier are softly commutated. A similar operation occurs in the reverse mode, only load, and supply voltage changes.

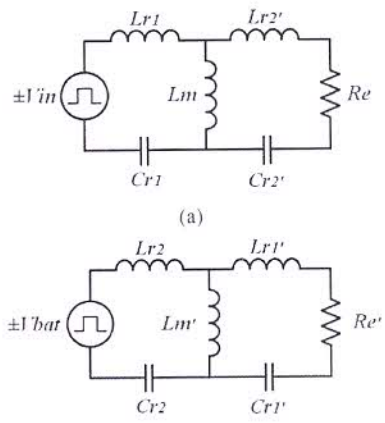

Fig. 4 FHA derived model of *CLLC* resonant converter for (a) Charging mode (CM) and (b) Discharging mode (DM)

B. Gain Analysis of CLLC Resonant Converter

i. Equivalent Circuit of CLLC converter while charging (CM)

The equivalent circuit of the *CLLC* converter in the charging mode is shown in Fig. 4(a) Assuming that 'n' is the transformer's turns ratio. Using the FHA, equivalent load resistance R_e can be expressed as follows [2][5].

$$R_e = \frac{8n^2}{\pi^2} R_o \tag{1}$$

Where, R_o is the actual load resistance in CM .

The secondary side resonant elements are referred to primary side and are shown in (2)

$$L'_{r2} = n^2 L_{r2}, C'_{r2} = \frac{C_{r2}}{n^2}, \tag{2}$$

The normalized frequency, quality factor, and the resonant frequency are shown in (3)

$$\omega = \frac{\omega_s}{\omega_r}, Q_f = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{R_e}, \omega_r = \frac{1}{\sqrt{L_{r1} C_{r1}}} \tag{3}$$

ii. Equivalent Circuit of CLLC converter while discharging (DM)

The Equivalent circuit of the *CLLC* converter in reverse mode is shown in Fig. 4(b), similar to (1) the equivalent load resistance (R_e') can be calculated using FHA [2][5] and is shown in (4)

$$R_e' = \frac{8}{n^2 \pi^2} R'_o \tag{4}$$

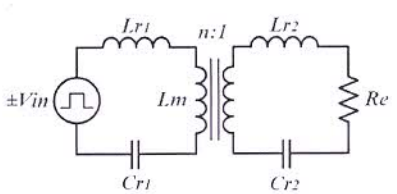

Fig. 5 Equivalent circuit of *CLLC* resonant converter with square wave source and equivalent AC resistance

Where, R'_o is the actual load resistance in DM. Similarly, the primary side resonant elements are referred to secondary side and are shown in (5)

$$L'_{r1} = \frac{L_{r1}}{n^2}, C_{r1} = n^2 C_{r1}, \omega_r = \frac{1}{\sqrt{L_{r2}C_{r2}}}$$

$$Q_r = \frac{\sqrt{\frac{L_{r2}}{C_{r2}}}}{R_{e'}}, \; L'_m = \frac{L_m}{n^2} \tag{5}$$

iii. Transfer function of the CLLC resonant converter

The general transfer function $H(s)$ can be derived by analyzing Fig. 5 in fourier domain and is expressed in (6)

$$H(s) = \frac{nVout}{Vin} = \frac{R_e(R_2//sL_m)}{R_2(sL_{r1}+\frac{1}{sC_{r1}}+R_2 sL_m)} = \frac{Vin}{\left(\frac{1}{sC_{r1}}+sL_{r1}\right)+\left(n^2 sL_{r2}+\frac{n^2}{sC_{r2}}+\frac{8n^2}{\pi^2}R_o\right)\left[1+\frac{1}{sL_m}\left(\frac{1}{sC_{r1}}+sL_{r1}\right)\right]} \tag{6}$$

Where,

$$R_2 = R_e + sn^2 L_{r2} + \frac{n^2}{sC_{r2}} \tag{7}$$

The gain function of *CLLC* converter in the forward mode is derived in [5], which could be expressed as (8)

$$|H(s)|_f = \frac{nV_{out}}{V_{in}} = \frac{1}{\sqrt{\left(\left(\frac{1}{h}-\frac{1}{h\omega^2}+1\right)^2+\left[\frac{1}{\omega}\left(\frac{m}{h}+\frac{1}{hg}+\frac{1}{g}+1\right)Q_f-\omega\left(\frac{m}{h}+m+1\right)Q_f-\frac{Q_f}{hg\omega^3}\right]^2\right)}} \tag{8}$$

Where,

$$h = \frac{L_m}{L_{r1}}, m = \frac{n^2 L_{r2}}{L_{r1}}, g = \frac{C_{r2}}{n^2 C_{r1}}$$

Similarly, the gain function for reverse mode can be expressed as in (9)

$$|H(s)|_r = \frac{1}{\sqrt{\left(\left(\frac{1}{p}-\frac{1}{p\omega^2}+1\right)^2+\left[\frac{1}{\omega}\left(\frac{r}{p}+\frac{1}{pq}+\frac{1}{q}+1\right)Q_r-\omega\left(\frac{r}{p}+r+1\right)Q_r-\frac{Q_r}{pq\omega^3}\right]^2\right)}} \tag{9}$$

Where,

$$p = \frac{L_m}{n^2 L_{r2}}, r = \frac{L_{r1}}{n^2 L_{r2}}, q = \frac{n^2 C_{r1}}{C_{r2}}$$

III. Design Methodology

A. Design of the Resonant Tank for CLLC converter

1. First, a resonant frequency is chosen considering the trade-offs between EMI, power density, and efficiency, too low resonant frequency can cause severe EMI issues [14]. For this design, the resonant frequency is selected as 350 kHz for CM and 300 kHz for DM.
2. Input and Output voltages of the converter is determined. Turns ratio of the transformer is selected via nominal input and output voltages (10)
3. MOSFETs are selected on the basis of frequency and gate charge requirements. For primary side, GaN devices from GaN systems are opted due to their reduced Figure of Merit (FOM) and high frequency operation.
4. For first iteration, L_n is kept at 5
5. Using a MATLAB script, required versus available gain is sweeped for different values of Q factor, shown in Fig. 6 This plot gives the frequency cut-off points for the converter.
6. A curve that fulfills the gain requirements is selected
7. The load resistance is converter to equivalent resistance seen by the AC source using (1) for CM and using (4) for DM.
8. (11,12) are used to calculate the required resonant inductance and capacitance.
9. Based on L_{r1} and L_n the magnetizing inductance is calculated L_m.
10. Value of L_m is must be less than the critical value of L_m to achieve zero voltage switching (ZVS) given by (13)

$$n = \frac{V_{in}}{V_{out}} = \frac{400}{48} = 8.33 \tag{10}$$

$$C_{r1} = \frac{1}{2\pi f_r Q_f R_e} \tag{11}$$

$$L_{r1} = \frac{1}{2\pi {f_r}^2 C_{r1}} \tag{12}$$

$$L_m \leq \frac{T_d}{16 C_{tr} F_M} \tag{13}$$

Where T_d is the deadtime period, C_{tr} is time related output capacitance of the MOSFETs, and F_M is the maximum switching frequency. Q factor for this design is selected such as it gives a desired linear range of operation simultaneously meeting the gain requirements. The AC resistance R_e in CM is 4.8Ω and 400Ω in DM. 3D mesh plots are depicted in Fig. 7 which provides a better overview of gain curves. The L_n is selected to be 5 as it facilitates a monotonic gain region and an optimal L_m to achieve ZVS. Table. I summarizes the resonant tank parameters for *CLLC* resonant converter.

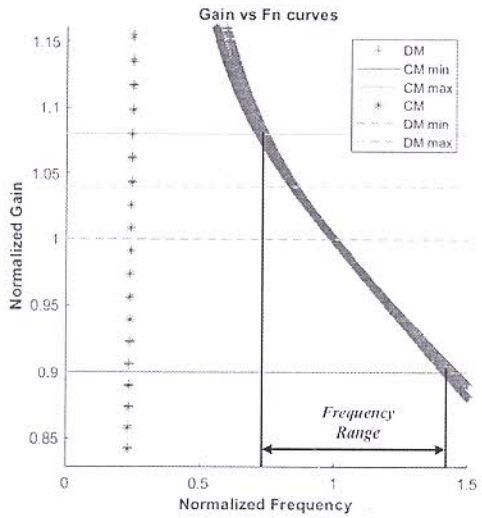

Fig. 6 MATALB plots for the CM and RM modes showing the linear region of operation

Fig. 6 Demonstrates the gain curves for CM/RM modes respectively, it also depicts the linear range of frequency modulation for the *CLLC* converter, which facilitates to implement linear compensators like PI/2P2Z etc.

TABLE I. Key Design Parameters of *CLLC* Converter

Parameters	Forward	Reverse
Input Voltage	360-400V	40-60V
Output Voltage	40-60V	390V
Resonant frequency F_r (kHz)	350	300
Current Sensor secondary	LEM-HLSR-20P	
Current Sensor Primary	ACS-712-10AB	
Voltage Sensor Primary	MCP6022+ACPL-C78B-000E	
Voltage Sensor Secondary	MCP6022	
Primary resonant capacitor C_{r1}	$11nF$	
Secondary resonant capacitor C_{r2}	$1\mu F$	
Primary resonant inductance L_{r1}	$17\mu H$	
Secondary resonant inductance L_{r2}	$260nH$	
Magnetizing inductance L_m	$120\mu H$	
Turns Ratio	8.33:1	