Design of Bi-directional *CLLC* Resonant Converter with Planar Transformer and Synchronous Rectification for Energy Storage Systems

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***Abstract*— This paper presents the design of a bi-directional *CLLC* resonant converter for low-voltage energy storage systems (48V) applications. Usually the power desnity for such converters are low due to low switching frequency operation. Thus for first step the swithcing frequency is kept ~300-350 kHz to reduce the size of passives components, which facilitates the usage of planar transformers to enhance power density. Generally the current on LV side is high and to mitigate this a synchronous rectification (SR) scheme is devised. FEA analysis is performed to verify the design of planar transformer for peak flux density, core and copper losses. The SRs and control loop (PI) is implemented via a 32-bit Microcontroller (TMS320F28379D) for CC/CV control in charging mode (CM) and Dishcharging Mode (DM) respectively. This proof of concept prototype is verfified through a 700W hardware prototype using GaN MOSFETs at high voltage and Silicon MOSFETs at low voltage side; achieving an efficiency of 96.6% in CM and 96.4% In DM.**

Keywords—CLLC converter, Energy Storage System (ESS), Finite Element Analysis (FEA), Charging Mode (CM), Discharging Mode (DM), and Gallium Nitride (GaN)

I. INTRODUCTION

DESs are emerging as an alternative to conventional energy sources to some extent; comprising of renewable sources of energy like photovoltaic (PV) and wind energy systems (WECS). DES can effectively support the energy requirements during peak load hours and can supply surplus energy to the utility grid during peak off hours. In this regard, a bi-directional resonant *CLLC* converter is proposed for battery charging mode (BCM) and reverse mode (RM) employing integrated planar transformer and synchronous rectification. *CLLC* and DAB are two widely adopted topologies for bi-directional power conversion [1]; for DAB converter, soft-switching is a challenge at light load; thus require complex control like in [3] to compensate for light-load efficiency. *CLLC* converter employs a frequency modulation (FM) scheme to control the dynamics of the resonant tank and regulate output power. The most widely adopted bi-directional power converters only account for high voltage (HV) outputs [5][6].

The DC distribution systems require a bi-directional AC-DC converter, which consists of a non-isolated AC-DC converter (power factor correction) and an isolated DC-DC converter (IBDC), authors in [18] developed a bi-directional AC-DC converter for DC distribution systems. Fig. 1 shows an ESS converting power from a HV bus to LV batteries bi-directionally.

The *CLLC* and DAB are two widely adopted topologies for DC-DC bi-directional power conversion [4]; the soft-switching ability is challenging and is subject to load conditions in DAB converter thus, requires complex control to modulate the phase shifts like in [19][20].In constrast, the *CLLC* resonant converter can achieve soft-switching for full load range, despite using a very simple and easy to implement control scheme of frequency modulation (FM) [2][3][7].

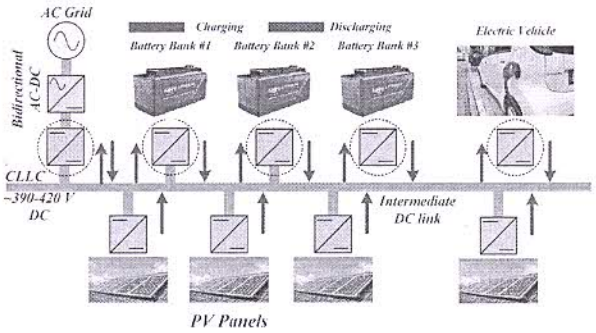


Fig. 1 *CLLC* resonant converter in a low voltage (LV) bus based Energy Storage System (ESS)

Apparantly most of the isolated bi-directional converters in [4-6][8-9] accounts for mostly high-voltage (HV) outputs and none LV outputs. In Indian scenario, the LV batteries are used for hybrid electric vehicle (HEVs), electric vehicle EVs and ESSs. In this regards, a bi-directional *CLLC* resonant converter is proposed to charge/Discharge LV batteries. The challenges in HV to LV power conversion is to deal with high output current in LV side which can cause severe conduction and termination loss. Thus, a synchronous rectification scheme is devised to enhance conversion efficiency. Section II discusses the theoretical analysis of the *CLLC* converter, the FHA derived model of *CLLC* converter, CM/DM mode analysis, and derivation of gain curves. Section III presents the design methodology of a *CLLC* resonant converter for battery charging application. Section IV presents the design of a planar transformer using analytical methods and FEA

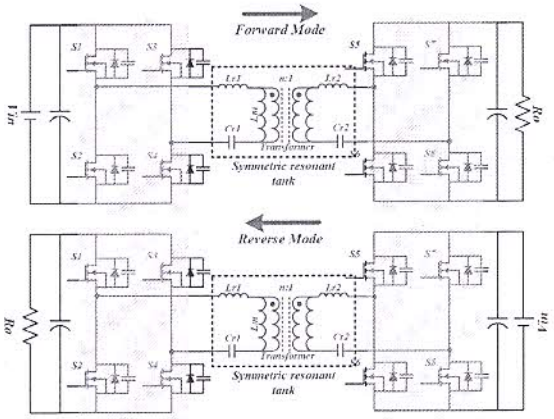


Fig. 2 Topology of *CLLC* resonant converter in charging (CM) and discharging (DM) modes

simulations. Section V presents a synchronous rectification methodology for full bridge *CLLC* resonant converter. Section VI discusses the control system for CC/CV charging of LV batteries. Ultimatley, the section VII concludes the design of a *CLLC* resonant converter by depicting simulation and hardware steady state/dynamic results.

II. THEORETICAL ANALYSIS OF *CLLC* RESONANT CONVERTER

Fig. 3 illustrates the waveforms for steady stage operation of the *CLLC* resonant converter operating below the resonant frequency.

A. Operation Modes of a CLLC Resonant Converter

Mode I represent a deadtime duration, during which all switches are turned off and no power is transferred to the secondary rectifying stage. The primary resonant current I_{Lr}, charges output capacitance of S_3, S_4 and discharges the output capacitance of S_1, S_2. After this process, the primary current passes through the anti-parallel diode of S_1 and S_2 which makes the switches operate under ZVS.

In II mode S_1, S_2 turns on and power is transferred through the transformer. The I_{Lr} reverses its direction to positive according to S_1, S_2 because the input source forces the current to positive direction through S_1, S_2, the output voltage from the secondary is impressed on the magnetizing inductance L_m, then the magnetizing current I_{Lm} , builds up linearly. Therefore, L_m does not participate in the resonance of the primary stage.

In mode III I_{Lr} equals magnetizing current, at this instant, the power transfer is stopped. Therefore, the secondary current I_s becomes zero, and the output capacitor is not charged by the output current. The I_{Lm} will keep rising till S_1, S_2 are turned off. During this mode, the L_m is no longer clamped by the output voltage. Thus, L_r, C_r and L_m participates in resonance together, and the resonant frequency of this mode is slightly different from other modes.

Mode IV is also a deadtime duration with the switch pair S_3, S_4. The operation is much similar to the mode I; however, the sequence of charging and discharging switches pair is different. The I_{Lr} discharges the output capacitances of S_3, S_4 and charges the output capacitances of S_1, S_2; and S_4, S_5 can turn on with ZVS.

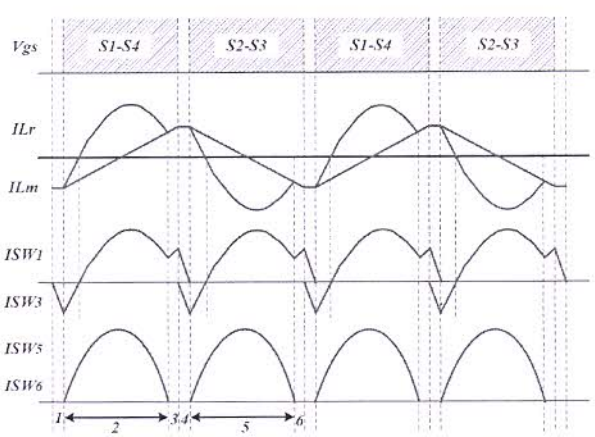


Fig. 3 Operating modes of the *CLLC* resonant converter operating below resonance

In mode V S_3, S_4 turn on and starts transferring power to the secondary side. During this mode, the I_{Lr} changes direction due to the impressed voltage but now in the opposite direction to that in mode II.

After the execution of Mode 5, the resonance and power transfer stops. With no power, the I_s becomes zero and the anti-parallel didoes of output rectifier are softly commutated. A similar operation occurs in the reverse mode, only load, and supply voltage changes.

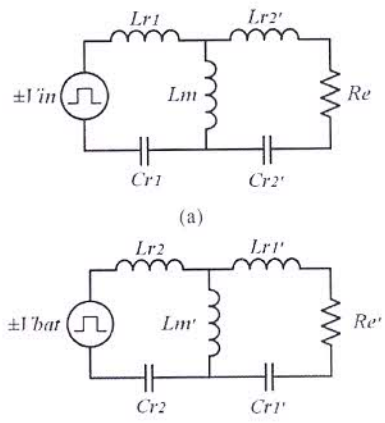


Fig. 4 FHA derived model of *CLLC* resonant converter for (a) Charging mode (CM) and (b) Discharging mode (DM)

B. Gain Analysis of CLLC Resonant Converter

i. Equivalent Circuit of CLLC converter while charging (CM)

The equivalent circuit of the *CLLC* converter in the charging mode is shown in Fig. 4(a) Assuming that 'n' is the transformer's turns ratio. Using the FHA, equivalent load resistance R_e can be expressed as follows [2][5].

$$R_e = \frac{8n^2}{\pi^2} R_o \tag{1}$$

Where, R_o is the actual load resistance in CM .

The secondary side resonant elements are referred to primary side and are shown in (2)

$$L'_{r2} = n^2 L_{r2}, C'_{r2} = \frac{C_{r2}}{n^2}, \tag{2}$$

The normalized frequency, quality factor, and the resonant frequency are shown in (3)

$$\omega = \frac{\omega_s}{\omega_r}, Q_f = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{R_e}, \omega_r = \frac{1}{\sqrt{L_{r1} C_{r1}}} \tag{3}$$

ii. Equivalent Circuit of CLLC converter while discharging (DM)

The Equivalent circuit of the *CLLC* converter in reverse mode is shown in Fig. 4(b), similar to (1) the equivalent load resistance (R_e') can be calculated using FHA [2][5] and is shown in (4)

$$R_e' = \frac{8}{n^2 \pi^2} R'_o \tag{4}$$

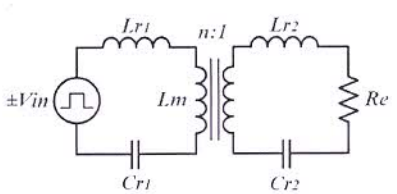


Fig. 5 Equivalent circuit of *CLLC* resonant converter with square wave source and equivalent AC resistance

Where, R'_o is the actual load resistance in DM. Similarly, the primary side resonant elements are referred to secondary side and are shown in (5)

$$L'_{r1} = \frac{L_{r1}}{n^2}, C_{r1} = n^2 C_{r1}, \omega_r = \frac{1}{\sqrt{L_{r2}C_{r2}}}$$

$$Q_r = \frac{\sqrt{\frac{L_{r2}}{C_{r2}}}}{R_{e'}}, \; L'_m = \frac{L_m}{n^2} \tag{5}$$

iii. Transfer function of the CLLC resonant converter

The general transfer function $H(s)$ can be derived by analyzing Fig. 5 in fourier domain and is expressed in (6)

$$H(s) = \frac{nVout}{Vin} = \frac{R_e(R_2//sL_m)}{R_2(sL_{r1}+\frac{1}{sC_{r1}}+R_2 sL_m)} = \frac{Vin}{\left(\frac{1}{sC_{r1}}+sL_{r1}\right)+\left(n^2 sL_{r2}+\frac{n^2}{sC_{r2}}+\frac{8n^2}{\pi^2}R_o\right)\left[1+\frac{1}{sL_m}\left(\frac{1}{sC_{r1}}+sL_{r1}\right)\right]} \tag{6}$$

Where,

$$R_2 = R_e + sn^2 L_{r2} + \frac{n^2}{sC_{r2}} \tag{7}$$

The gain function of *CLLC* converter in the forward mode is derived in [5], which could be expressed as (8)

$$|H(s)|_f = \frac{nV_{out}}{V_{in}} = \frac{1}{\sqrt{\left(\left(\frac{1}{h}-\frac{1}{h\omega^2}+1\right)^2+\left[\frac{1}{\omega}\left(\frac{m}{h}+\frac{1}{hg}+\frac{1}{g}+1\right)Q_f-\omega\left(\frac{m}{h}+m+1\right)Q_f-\frac{Q_f}{hg\omega^3}\right]^2\right)}} \tag{8}$$

Where,

$$h = \frac{L_m}{L_{r1}}, m = \frac{n^2 L_{r2}}{L_{r1}}, g = \frac{C_{r2}}{n^2 C_{r1}}$$

Similarly, the gain function for reverse mode can be expressed as in (9)

$$|H(s)|_r = \frac{1}{\sqrt{\left(\left(\frac{1}{p}-\frac{1}{p\omega^2}+1\right)^2+\left[\frac{1}{\omega}\left(\frac{r}{p}+\frac{1}{pq}+\frac{1}{q}+1\right)Q_r-\omega\left(\frac{r}{p}+r+1\right)Q_r-\frac{Q_r}{pq\omega^3}\right]^2\right)}} \tag{9}$$

Where,

$$p = \frac{L_m}{n^2 L_{r2}}, r = \frac{L_{r1}}{n^2 L_{r2}}, q = \frac{n^2 C_{r1}}{C_{r2}}$$

III. Design Methodology

A. Design of the Resonant Tank for CLLC converter

1. First, a resonant frequency is chosen considering the trade-offs between EMI, power density, and efficiency, too low resonant frequency can cause severe EMI issues [14]. For this design, the resonant frequency is selected as 350 kHz for CM and 300 kHz for DM.
2. Input and Output voltages of the converter is determined. Turns ratio of the transformer is selected via nominal input and output voltages (10)
3. MOSFETs are selected on the basis of frequency and gate charge requirements. For primary side, GaN devices from GaN systems are opted due to their reduced Figure of Merit (FOM) and high frequency operation.
4. For first iteration, L_n is kept at 5
5. Using a MATLAB script, required versus available gain is sweeped for different values of Q factor, shown in Fig. 6 This plot gives the frequency cut-off points for the converter.
6. A curve that fulfills the gain requirements is selected
7. The load resistance is converter to equivalent resistance seen by the AC source using (1) for CM and using (4) for DM.
8. (11,12) are used to calculate the required resonant inductance and capacitance.
9. Based on L_{r1} and L_n the magnetizing inductance is calculated L_m.
10. Value of L_m is must be less than the critical value of L_m to achieve zero voltage switching (ZVS) given by (13)

$$n = \frac{V_{in}}{V_{out}} = \frac{400}{48} = 8.33 \tag{10}$$

$$C_{r1} = \frac{1}{2\pi f_r Q_f R_e} \tag{11}$$

$$L_{r1} = \frac{1}{2\pi {f_r}^2 C_{r1}} \tag{12}$$

$$L_m \leq \frac{T_d}{16 C_{tr} F_M} \tag{13}$$

Where T_d is the deadtime period, C_{tr} is time related output capacitance of the MOSFETs, and F_M is the maximum switching frequency. Q factor for this design is selected such as it gives a desired linear range of operation simultaneously meeting the gain requirements. The AC resistance R_e in CM is 4.8Ω and 400Ω in DM. 3D mesh plots are depicted in Fig. 7 which provides a better overview of gain curves. The L_n is selected to be 5 as it facilitates a monotonic gain region and an optimal L_m to achieve ZVS. Table. I summarizes the resonant tank parameters for *CLLC* resonant converter.

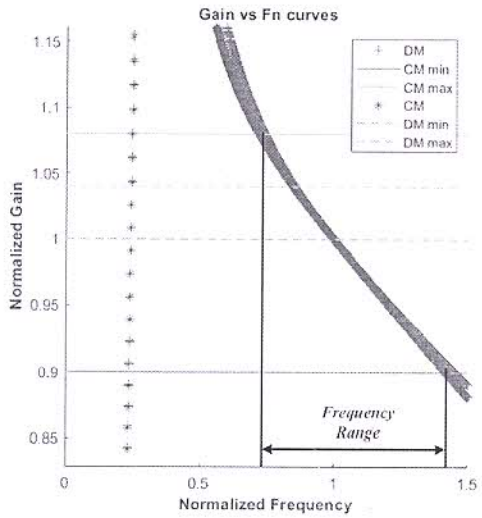
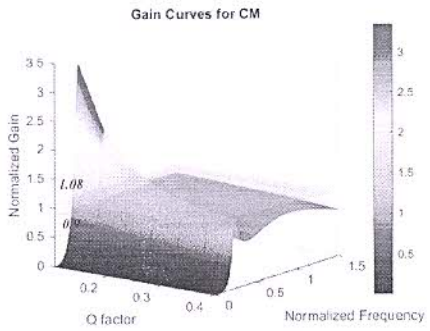


Fig. 6 MATALB plots for the CM and RM modes showing the linear region of operation

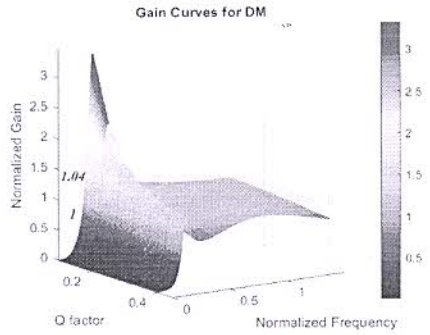
Fig. 6 Demonstrates the gain curves for CM/RM modes respectively, it also depicts the linear range of frequency modulation for the *CLLC* converter, which facilitates to implement linear compensators like PI/2P2Z etc.

TABLE I. Key Design Parameters of *CLLC* Converter

Parameters	Forward	Reverse
Input Voltage	360-400V	40-60V
Output Voltage	40-60V	390V
Resonant frequency F_r (kHz)	350	300
Current Sensor secondary	LEM-HLSR-20P	
Current Sensor Primary	ACS-712-10AB	
Voltage Sensor Primary	MCP6022+ACPL-C78B-000E	
Voltage Sensor Secondary	MCP6022	
Primary resonant capacitor C_{r1}	$11nF$	
Secondary resonant capacitor C_{r2}	$1\mu F$	
Primary resonant inductance L_{r1}	$17\mu H$	
Secondary resonant inductance L_{r2}	$260nH$	
Magnetizing inductance L_m	$120\mu H$	
Turns Ratio	8.33:1	



(a)

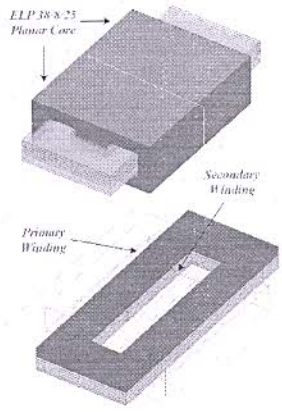


(b)

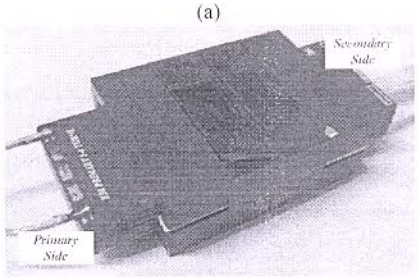
Fig. 7 3D MATLAB plots of converter gain for (a) CM gain is 0.9-1.08 (b) DM gain is 1-1.04 for *CLLC* resonant converter

IV. Design of Planar Transformer and FEA Simulation Results

In order to achieve high power density and reduce converter volume it is required to have a high switching frequency. Conventionally with a low frequency design (~50-80 kHz) it is obligatory to have a separate resonant choke/inductor as the require leakage inductance cannot be fulfilled by the leakage in the transformer. Thus, one benefit of HF operation is that a modicum of resonant inductance is required which can be easily delivered by either a traditional wire wound (WW) or planar magnetics. But the benefit of planar transformer over WW transformer is that the leakage can be controlled in much better way compared to the WW where manipulating leakage is almost impossible. On contrary, leakage of a planar transformer can be manipulated via changing the gap between two layers of primary and secondary. High Frequency operation cause several losses like skin effect, proximity loss due to increase AC resistance caused by skin effect and non-uniform distribution of AC in transformer winding due to proximity effect, respectively. Skin effect can be avoided by incorporating a conductor whose diameter is about or small than the skin depth at a particular frequency the expression for skin depth is given by (15). PCB windings play a key role in nearly eliminating skin effect as the thickness of copper is nearly or less than the skin depth of copper. Both primary and secondary windings are made of PCB stacks. Proximity effect can be reduced by interleaving the primary and secondary windings but, it results in reduction of leakage inductance which is required to act as resonant inductor. Thus, in this design, interleaving is not possible rather a leakage gap l_b is introduced between primary and secondary windings so as to increase the leakage inductance to a desired value. Compared to the litz wire based winding structure, PCB based winding

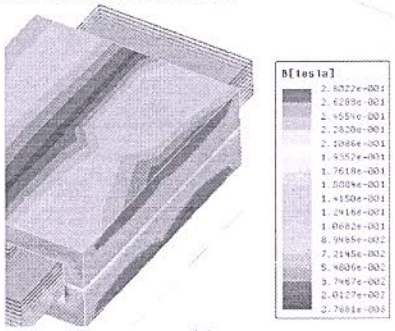


(a)



(b)

Fig. 8 (a) 3D model of PCB stack based planar transformer (b) developed PCB stack based transformer



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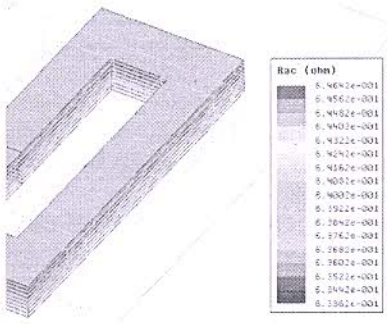

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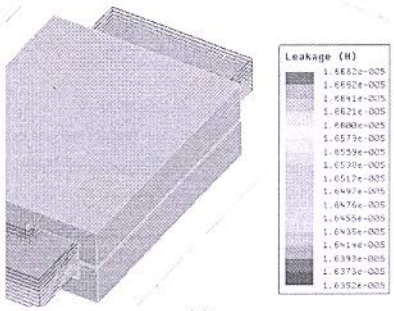


(c)

Fig. 9 FEA simulation results for (a) peak magnetic flux density in core material (b) AC resistance of PCB windings at 350 kHz (c) lekage inductance at 350 kHz

structures are susceptible to high frequency AC winding loss [15] due to skin effect. Considering the 1D model as per [21].

$$\begin{cases} F_R = \frac{R_{AC}}{R_{DC}} = M' + \frac{(m^2-1)D'}{3} \\ M = \delta h \coth \delta h \\ D = 2\delta h \tanh \delta h/2 \end{cases} \quad (14)$$

$$\begin{cases} \delta = \sqrt{\frac{j\omega\mu_o\eta}{\rho}} \\ \eta = \frac{aN_l}{b} \end{cases} \quad (15)$$

Where, F_R is the ratio of AC winding resistance to the DC winding resistance, M', D' are the real parts of M and D, h is the height of the conductor (which in this case is the thickness of copper in PCB), μ_o is the permeability of free space, a is the width of the conductor, Nl is the number of turns per layer, and b is the window width. Using the above equations, F_R can be calculated as 3.579. Thus, the AC resistance of windings can be calculated as:

$$R_{AC} = F_R R_{DC} \quad (16)$$

PCB of copper thickness 2Oz is used for for primary and secondary windings and secondary windings are paralleled for high current output. To avoid saturation an air gap is placed between the legs of ELP core. Table. II shows the key parameters of an integrated planar transformer.

TABLE II. KEY PARAMETERS OF INTEGRATED PLANAR TRANSFORMER

Parameters	Value
Turns ratio Np: Ns	7.5:1
Core Size	ELP 38/8/25 -2
Core material	3F4
Leakage air gap (mm)	0.9
Core air gap (mm)	0.7

Considering power requirements 2-ELP 38/8/25 planar E core from Ferroxcube is opted to have sufficient winding area and leakage inductance. A core material is selected such that it allows a switching frequency of 290-370 kHz and do not cause severe core loss, 3F4 from Ferroxcube is used as core material which has a peak flux density of 0.4T. Fig. 8 shows the (a) PCB stacks for primary and secondary windings in a 3D model and (b) actual tr. Fig. 9 depicts the FEA simulation results for (a) peak flux density (b) AC resistance and (c) leakage inductance. Fig. 10 shows (a) MMF distribution among windings (b) ELP38/8/25 core. Table. III shows the FEA calculated versus measured parameters for transformer.

TABLE III. MEASURED AND FEA SIMULATED PARAMETERS OF PROPOSED INTEGRATED TRANSFORMER

Parameters	Measured	FEA Simulated
Leakage Inductance Primary	17 μH	16.5 μH
Leakage Inductance Secondary	314 nH	220 nH
AC resistance Primary	627 $m\Omega$	650 $m\Omega$
AC resistance Secondary	10.62 $m\Omega$	11.54 $m\Omega$

V. SYNCHRONOUS RECTIFICATION FOR FULL-BRIDGE *CLLC* RESONANT CONVERTER

Due to lagging current in the resonant tank, there exists a natural phase difference between gate pulses of primary and resonant current of secondary side. This phase difference can be denoted by Δd and is dependent on resonant tank elements

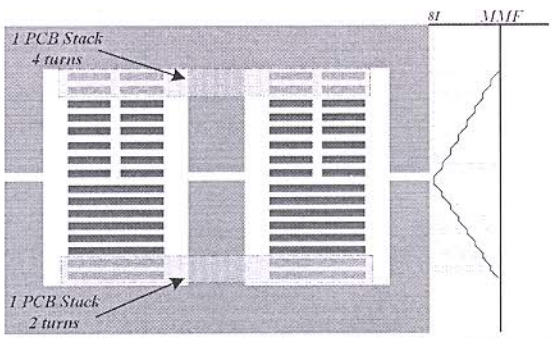


Fig. 10 MMF distitbution among primary and secondary windings of the proposed planar transformer

and operating frequency [9][10]. This phase difference can be measure via turning off SRs and only using body diodes of the secondary MOSFETs. Switches on the secondary side must be synchronized with the resonant current of the secondary side. If turn-on timing is not synchronized properly, then there would be circulating currents in the secondary windings which would furter increase the conduction loss and thus the efficiency. Fig. 11 (a) shows the body diode conduction path (no circulation loss) (b) shows the conduction path of the circulating current if SRs are not engaged properly as per the polarity of the secondary-side resonant current. Authors in [22] proposed a method to execute SR operation for high-frequency applications.

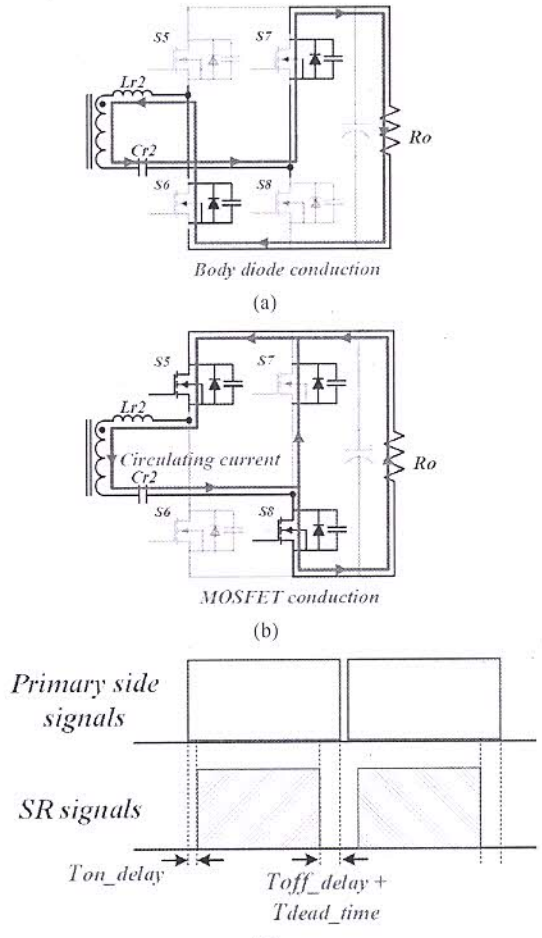


Fig. 11 (a) body diode conduction and no circulation loss (b) mis-triggering of SRs and circulation loss in secondary winding (c) proposed SR control which incorporates turn-on and turn-off delays

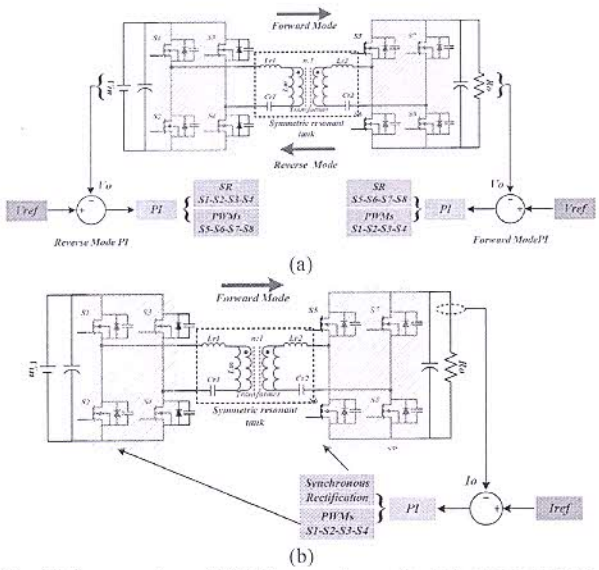


Fig. 12 Compensators of *CLLC* resonant converter (a) voltage control loop in both CM/DM (b) current control loop in CM

VI. CONTROL SYSTEM FOR CC/CV CHARGING-DISCHARGING

Designing a resonant converter for fixed output voltage is somewhat less taxing than designing it for a battery charging application where the voltage of a battery varies as its state of the charge (SOC) changes. Thus, it is difficult to design a *CLLC* resonant converter with wide output voltage range without sacrificing conversion efficiency, this design would include a contribution on the part of AC-DC PFC converter but in this paper, only the design of DC-DC part is discussed.

To keep control system quite simple, a widely used frequency modulation (FM) scheme is used to control the *CLLC* resonant converter. FM is widely adopted for LLC resonant converter for uni-directional charging and most of the resonant converters as well. Here in this design FM is used to achieve constant current (CC) and constant voltage (CV) charging in CM and DM, respectively. In section III the gain curves depicts that a linear range of operation is utilized for this design which aids to use a linear compensator like PI for CC/CV charging. The transfer fucnction of PI is given by (17)

$$C(s) = K_p + \frac{K_i}{s} \tag{17}$$

Increasing K_p may result in faster dynamic response, but jeopardizes the phase margin and thus stability of the control loop. Equation (6) can be used to derive the expression for output voltage $V_o(s)$; a partial derivative with respect to the variable s would give a plant transfer function $T_P(s)$ as of in [12] which can be derived as (18)

$$T_P(s) = \frac{\partial V_o(s)}{\partial s} =$$

$$\frac{8n^2 R_o V_{in}}{\pi^2} \frac{\frac{1}{s^2 C_{r1}} - L_{r1} + \frac{n^2 L_{r2} - \frac{n^2}{s^2 C_{r2}}}{s^3 L_m C_{r1}}}{\left\{\left(\frac{1}{sC_{r1}} + sL_{r1}\right) + \left(n^2 sL_{r2} + \frac{n^2}{sC_{r2}} + \frac{8n^2}{\pi^2} R_o\right)\left[1 + \frac{1}{sL_m}\left(\frac{1}{sC_{r1}} + sL_{r1}\right)\right]\right\}^2} \tag{18}$$

Multiplying the plant transfer function by PI compensator's transfer function gives the loop gain of the control system. The closed-loop transfer function of the control system $G(s)$ can be derived as (19)

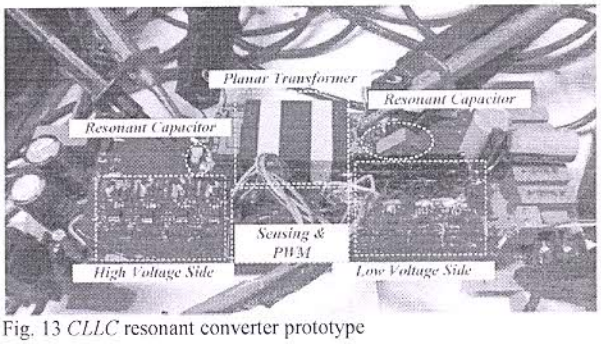


Fig. 13 *CLLC* resonant converter prototype

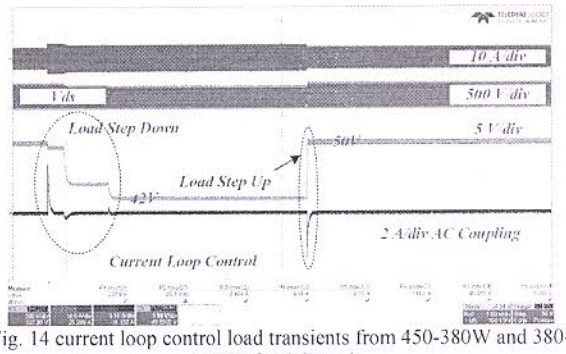


Fig. 14 current loop control load transients from 450-380W and 380-450W for CC mode

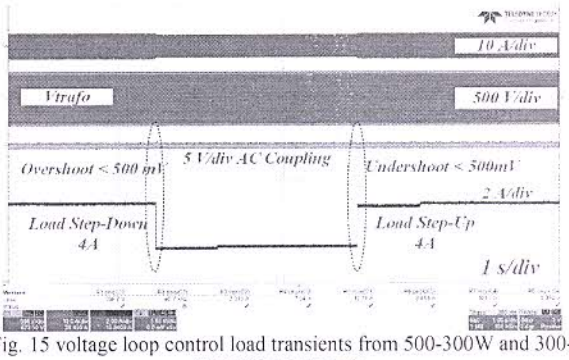
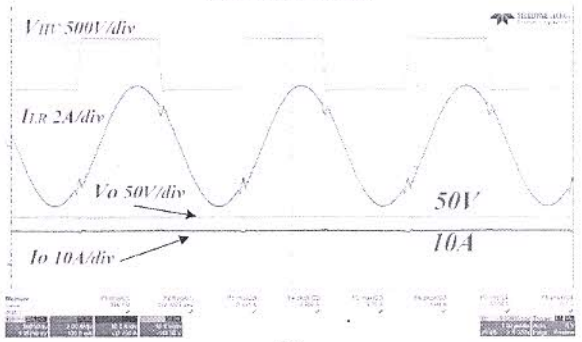
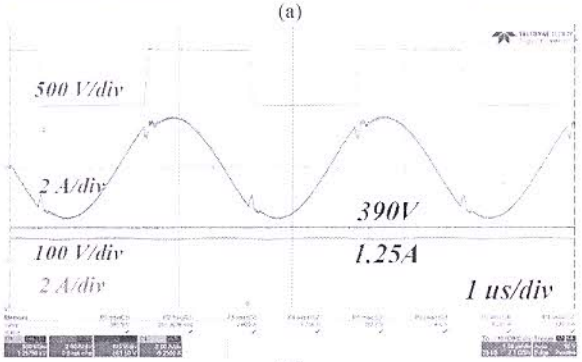


Fig. 15 voltage loop control load transients from 500-300W and 300-500W for CV mode



(a)



(b)

Fig. 16 Steady state waveforms for *CLLC* resonant converter (a) in charging mode at 500W output (b) in discharging mode at 500 W output

$$G(s) = \frac{C(s)T_P(s)}{1+C(s)T_P(s)} = \frac{K_p+\frac{K_i}{s}}{K_p+\frac{K_i}{s}+\frac{\pi^2\left\{\left(\frac{1}{sC_{r1}}+sL_{r1}\right)+\left(n^2sL_{r2}+\frac{n^2}{sC_{r2}}+\frac{8n^2}{\pi^2}R_o\right)\left[1+\frac{1}{sL_m\left(\frac{1}{sC_{r1}}+sL_{r1}\right)}\right]\right\}^2}{8n^2R_oV_{in}\left(\frac{1}{s^2C_{r1}}-L_{r1}+\frac{n^2L_{r2}-\frac{n^2}{s^2C_{r2}}}{s^3L_mC_{r1}}\right)}} \quad (19)$$

Where, $C(s)$ is the transfer function of the PI controller. The PI controller is implemented in a 32-bit digital microcontroller (TMS320F28379D). Fig. 12 (a) shows the voltage loop control and current loop control of the *CLLC* converter while charging and discharging (b) shows the current loop control of the *CLLC* converter while charging. Only the voltage loop control is considered while discharging; as the load may not be a stiff voltage source thus, needed to be maintained.

VII. Harware Results of *CLLC* Resonant Converter

A proof of concept prototype of GaN based *CLLC* resonant converter with planar transformer and synchronous rectification is designed, built, and tested for a maximum power of 700W with a switching frequency of 350 kHz in CM and 300 kHz in DM and is shown in Fig. 13. Control loop for CC/CV mode transitions for CM are depicted in Fig. 14 where power in CC mode varies from 450W-380W and 380W-450W and in CV mode it varies from 500W-300W and 300W-500W, respectively. Fig. 15 depicts the CV transient in DM. Fig. 16 (a,b) shows the steady state waveforms for *CLLC* resonant converter in CM/DM. One of the major benefits of using GaN devices is the better thermals than silicon, due to low thermal resistance from junction to case R_{thjc} heat is dissipated quickly via PCB or a small heatsink. In this design no heatsink was used on high voltage GaN devices, Fig. 17 shows the thermal profile of the converter. Individual loss elements in the converter are identified and are summarized in a forms of graph in Fig. 18 . Most loss occurs in the core due to reason that material is on lower threshold of its frequency limit, the core loss density would decrease only if the frequency get above 500 kHz, which is not possible due to the silicon MOSFETs deployed on low voltage side, thus the core loss is the only significant loss element in this design. Fig. 19 depicts the conversion efficiency of the *CLLC* resonant converter for charging (CM) and discharging operation (DM), respectively. Fig. 20 shows the test bench setup for the *CLLC* resonant converter in CM/DM operations.

VIII. Conclusion

In this paper the design of a *CLLC* resonant converter with planar transformer and synchronous rectifiers is presented and discussed. The resonant tank is optimized to be controller via linear compensator like PI. An integrated planar transformer is designed to accommodate the leakage inductance as resonant inductor, this transformer also helps in achieving high power density. The current on low voltage side is usually high which could cause severe conduction losses if only diodes are used for rectification. Instead Syncronous rectification is used for low voltage side, therby reducing the conduction losses by significant amount. FM based control is implemented to achieve CC/CV charging for batteries and robustness of control is depicted via load

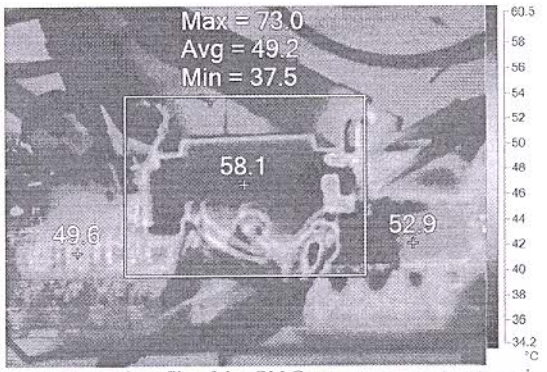


Fig. 17 Thermal profile of the *CLLC* resonant converter at maximum power of 700W

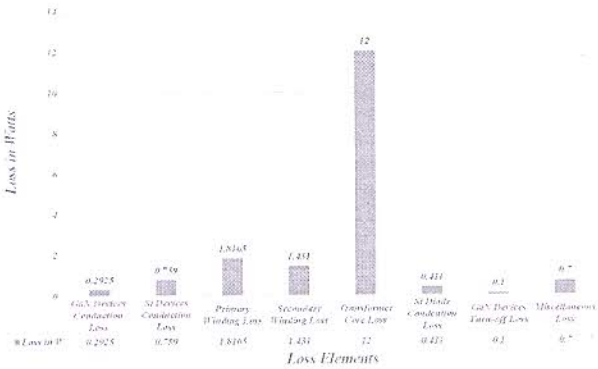


Fig. 18 Loss elements in *CLLC* resonant converter, all elements are calculated except fot gate drive loss

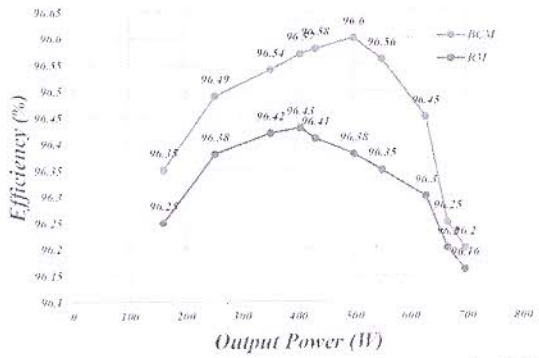


Fig. 19 Conversion efficiency of *CLLC* resonant converter in CM/DM operation, respectively

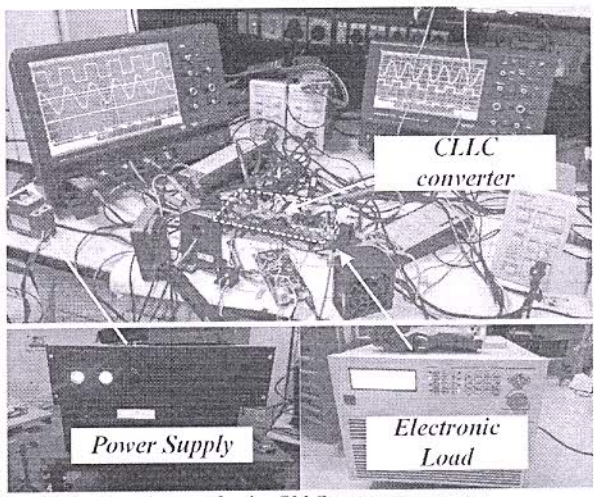


Fig. 20 Test bench setup for the *CLLC* resonant converter

transients. The converter achieves a peak efficiency of 96.6% in chargin mode (CM) and 96.4% in discharging mode (DM), respectively.

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