Topic | **III-Nitrides: Materials and Devices**

In-situ passivated GaN on Si HEMT for High voltage Applications

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GaN based HEMT devices are well known for their less frequency dependent switching losses, high breakdown electric field, high switching speed, high current density in high power and high frequency applications. GaN based HEMT on Si substrate provides a cost effective, reliable and highly manufacturable platform [1]. In this paper, we are reporting on the in-situ passivated GaN on silicon technology for various high voltage applications like Electrical vehicle automobile industry, aircraft electronics, satellite applications, electric motor controllers etc. [2]. The GaN on Si HEMT devices were fabricated for high voltage applications which consists of 650 μm thick silicon substrate, a GaN buffer layer of 3.9 μm epitaxially grown over substrate using MOCVD. This was followed by higher band gap material AlGaN (Al composition=0.25) of 20nm to generate the two-dimensional electron gas (2DEG) channel. In order to reduce gate leakage and to increase the Schottky barrier height a GaN cap layer of 2nm is also epitaxially grown followed by in-situ grown nitride passivation layer. The ohmic contacts were optimized and we achieved a very good contact resistivity of 2.5×10^{-6} ohm-cm^2 and a sheet resistance of 350 ohms/square followed by a very crucial step of passivation layer etching. Isolation process has been optimized using Boron, Nitrogen and Argon implant which results into a very good isolation resistance of 5×10^{10} Ohms/sq. at 100 volts (as shown in Fig. 1). A mobility of 1670 cm^2/V-sec and a carrier concentration of 1.286e+13 /cm^2 was measured using hall-effect measurement system. The fabricated GaN HEMT on Si showed a device saturated current (I_{DSS}) of 300 mA/mm at V_{gs}=2 volts and a peak trans conductance (G_m) of 110 mS/mm. 3-terminal Breakdown voltage was measured by biasing the gate near to pinch off. We achieved a breakdown voltage over 210 Volts (Resource limitation) in depletion mode (as shown in Fig. 2). Device survived without any sign of breakdown and can withstand even higher voltages.

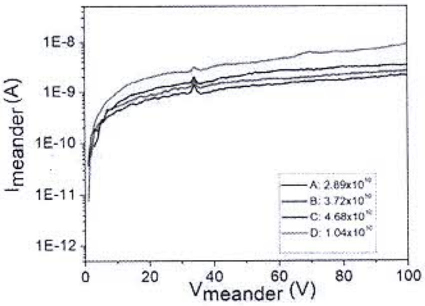

Fig.1: Isolation Resistance measurement of Device

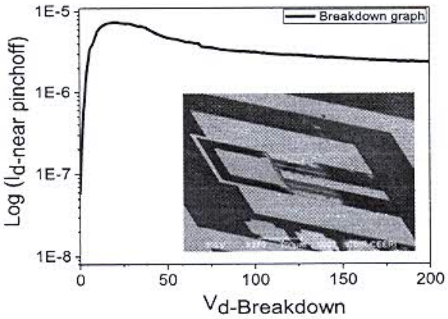

Fig.2: Breakdown characteristics and SEM image

References

[1] Chen, Kevin J., et al. "GaN-on-Si power technology: Devices and applications." *IEEE Transactions on Electron Devices*64.3 (2017): 779-795.

[2] Z. Zhang et al., "Studies on High-Voltage GaN-on-Si MIS-HEMTs Using LPCVD Si3N4as Gate Dielectric and Passivation Layer," in IEEE Transactions on Electron Devices, vol. 63, no. 2, pp. 731-738, Feb. 2016.