FPGA Based Implementation of Linear SVM for Facial Expression Classification

[1,2] Sumeet Saurav
[1]Academy of Scientific & Innovative Research
[2] CSIR-Central Electronics Engineering Research Institute
Pilani, India
sumeetssaurav@gmail.com

Ravi Saini, Sanjay Singh
IC Design Group
CSIR-Central Electronics Engineering Research Institute
Pilani, India
{ravi, sanjay}.csirceeri@gmail.com

Abstract— **This work presents a Field Programmable Gate Array (FPGA) based hardware efficient implementation of One-Versus-All (OVA) linear Support Vector Machine (SVM) classifier for classifying the facial expressions on an individual. The motivation is to achieve a real-time classification of the facial expressions of an individual into three different states viz., neutral, happy, and pain so that the designed architecture could be used as a part of an embedded platform based FER system for the purpose of monitoring patients in hospitals. Thus, the design challenge is to achieve classification accuracy equivalent to the software-based implementation with a multi-fold improvement in the execution time. The acceleration in the execution time of the designed classifier has been achieved utilizing the parallelism and pipelining concepts of the VLSI architecture design. Moreover, to reduce the computational cost and boost the execution speed of the architecture we have adopted the fixed-point data format (Q24.16) in our design. The classifier has been trained offline and the parameters of the trained classifier have been used to perform testing using the designed architecture on hardware. The designed architecture after synthesis operates at a maximum clock frequency of 241.55 MHz and is resource efficient. Classification accuracy of 98.50% equivalent to its software counterpart has been achieved on simulating the designed architecture with different test images. Thus, the designed classifier architecture shows good performance in terms of speed, area, and accuracy, and is suitable for real-time classification of the facial expressions.**

Keywords— Support Vector Machines, VLSI Architectures, FPGA, AdaBoost, Gabor filter.

I. INTRODUCTION

In today's world of automation, there has been a huge requirement of Facial Expression Recognition (FER) based technology and thus it has become an important area of research among the researchers of the Computer Vision community. The FER technology has a plethora of applications in areas related with human-computer interfaces; patient monitoring, blind person assistance; human emotion analysis [1]; neuroscience, psychology, and cognitive sciences [2]; access control and surveillance [3]; and communication, personality, and child development [4]. Moreover, recent rapid advancement in the Machine Learning and deep learning algorithms has further widened the areas of research in the design of an efficient FER system. However, designing such a system is not a trivial job because of a number of issues and researchers all around the world are trying to mitigate these issues and desired to have human-level performance in the FER based systems.

Over the decades, there have been numerous works reported in the literature dealing with the demonstration of FER system and its practical applications. However, most of these works have targeted towards enhancing the accuracy of these systems without keeping into consideration the real-time constraint which is often the desired requirement.

One of the most important ingredients of any FER system is the classification unit which is used to assign labels to different facial expressions and for this SVM classifier is often considered to the best candidate. Therefore, in this work, we have designed an optimal architecture of an OVA linear SVM classifier to facilitate real-time classification of the facial expressions of an individual.

Most of the available literature on SVM listed in [5]-[12], have discussed their software-based implementation. The first significant work related to the hardware-based implementation of SVM has been reported in [13]. A digital architecture for both the training and testing phase of the SVM using both linear and non-linear (RBF) kernels have been reported. Although, the designed architecture implemented on Xilinx Virtex-II FPGA fulfilled its objectives but suffers from two major drawbacks. Firstly, the FPGA resource utilization is too high and secondly, the processing speed (35.3 MHz) obtained is not acceptable for many applications demanding real-time performance. In order to overcome the issues of high FPGA resource utilization, the authors in [14] proposed a hardware-based SVM classification architecture targeted to FPGA using the Logarithmic Number System (LNS). The authors have claimed to save considerable hardware resources with no significant loss in classification accuracy, but difficulties lie in converting real numbers to their logarithmic equivalent representation. An FPGA friendly implementation of a Gaussian Radial Basis SVM well suited to the classification of grayscale images has been discussed in [15]. The implementation achieved 88.6% detection accuracy (equivalent to software-based implementation) in gender classification. A parallel hardware architecture based FPGA implementation of SVM for the video shot boundary detection application have been discussed in [16]. For brain-computer interface application, an FPGA based implementation of linear kernel support vector machines is reported in [17]. The authors have demonstrated that their hardware model achieved a