Zynq SoC Based High Speed Data Transfer Using PCIe: A Device Driver Based Approach

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***Abstract*— High Speed Data Transfers is a typical requirement of data intensive applications like image and video processing. Speed efficiency can be ensured by handling the data transfers at both Hardware and Software level. A complete system has been developed by implementing the hardware architecture on FPGA and writing corresponding Software device driver to perform the speedy data transfers from endpoint to a root complex device using PCIe interface. This paper describes the approach to design and verify this system. The speed of data transfer achieved practically for PCIe (2.0) x4 is 4Gib/s. The developed hardware architecture is resource constrained and low power. The hardware is implemented on Xilinx Zynq device. This work has a good potential in the field of image and video processing and can be used to perform large data transfer operations at high speed.**

Keywords*— *PCIe, Zynq, XMD, High Speed, DMA

I. Introduction

Image and video processing has revolutionized the world with its high performance digital cameras having flexible interface to achieve high throughput. The camera captured images are put to hardware accelerators to perform filtering, processing and displaying operations. There are huge number of computations performed on the captured images using FPGA boards. FPGA devices are used to create reconfigurable hardware architectures to perform the above said operations at high speed. After applying the image and video processing algorithms on the captured images, these images are sent to Central Processing Unit (CPU) for displaying and further processing. In this paper, a hardware architecture is developed in Xilinx Vivado using IPs to send the processed images data from the FPGA board to CPU with very low latency. Peripheral Component Interconnect Express (PCIe) is used here as the high speed serial interface to create the communication link between FPGA board and the CPU. To create and manage the PCIe interface, a software device driver is written on Linux Ubuntu OS which performs the data transfer operations smoothly and speedily [1].

For a typical high speed vision requirement, frames are captured at more than 250 frames/sec, pre-processed and sent to CPU for further processing and usage. A high speed frame grabber which captures image at more than 250 frames/sec with resolution of (512*512 pixels), needs a high speed (Gib/s) interface through which the data could be sent to the host system for further processing. In order to fulfill the high throughput need of high-speed digital data processing and to achieve high-speed communication between digital front-ends and computer, PCIe is the best suitable interface now a days [2]. This interface has a number of versions and lanes which could be used as per the application requirement. In this paper, PCIe (2.0) x4 is used to analyze the capability and efficiency of this interface. The developed hardware architecture is having Zynq SoC, which has abundant logic cells and dual hard core ARM Cortex A9 processors to make the complex decisions based on the arrived data from the peripherals like high speed camera. The Zynq SoC is also having the Programmable Logic (FPGA) and is capable in processing large data, applying massively parallel algorithms and performing speedy computations. Fig. 1 describes the interaction between PCIe endpoint and root complex CPU. Xilinx ZC706 board having Zynq-7000 all programmable SoC (Z-7045) is used as a PCIe endpoint.

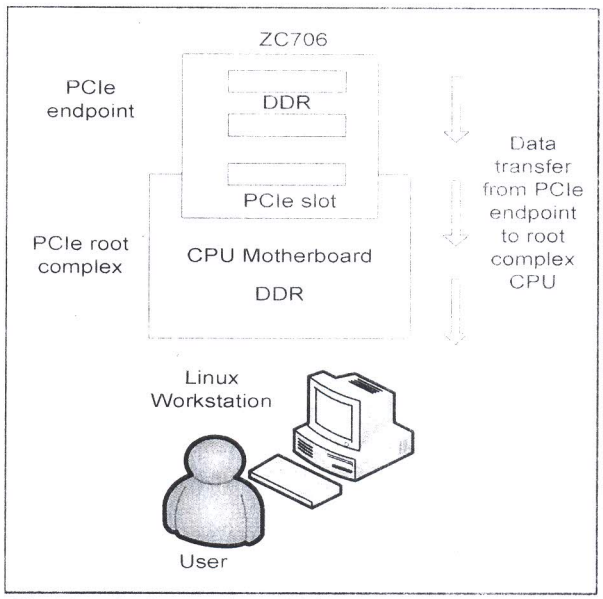

Fig. 1 Introduction to endpoint initiated data transfer through PCIe

ZC706 has PCIe (2.0) x4 interface, 1 GB DDR3 for processing systems (PS) and another 1 GB for Programmable Logic (PL). The hardware design is made using reconfigurable