An Improved Highly Efficient Low Input Voltage Charge Pump Circuit

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Abstract. Conventional charge pump circuit based on dynamic charge transfer switch (CTS) is limited by its efficiency due to the threshold voltage of MOS transistor. This paper proposes an improved dynamic CTS based charge pump circuit by modifying the conventional circuit architecture at the output stage by a PMOS transistor with appropriate control signals. A four-stage dynamic CTS based charge pump circuit with pumping capacitance of 50 pF, clock frequency of 20 MHz and load current of 100 µA is designed and simulated in Cadence environment using UMC 0.18 µm CMOS technology. As compared to conventional architecture, this modification has reduced the voltage loss at the output to 1.3% as compared to 9% for 1 V input and 6% as compared to 20% for 0.3 V input voltage. The core dimension of the layout is 750 µm × 530 µm.

Keywords: DC-DC converter, charge pump, CMOS.

1 Introduction

Charge pump (CP) circuits are capacitive DC-DC boost converters that provide a DC output voltage higher than the input supply voltage. Capacitive DC-DC converter circuits occupy less silicon area and can be fully integrated on-chip as compared to inductor based DC-DC converters. Recent developments in sub-micron technologies have scaled down the supply voltages. To combat the performance degradation of analog and mixed signal circuits due to reduced supply voltages, multiple supply strategy is implemented. This strategy meets both low power operation and high performance requirements in an integrated-chip (IC). However, CP circuits are also used in other applications for biasing sensors requiring higher voltage than the input supply voltage [1], programming of EEPROM [2, 3], fully-integrated energy harvesting circuits for boosting the voltage obtained from ambient sources [4, 5] etc. The first integrated CP circuit was proposed by Dickson [6]. CP circuit proposed by Dickson is simply a chain of series connected diode and capacitor. Further diodes were replaced with gate-drain connected MOS transistors for on-chip implementation.

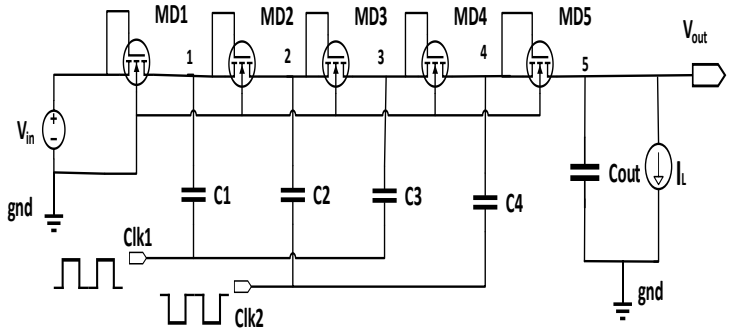

Fig. 1. Four stage Dickson charge-pump circuit [5].

Conventional architecture of the Dickson CP with MOS transistors is shown in Fig. 1. As shown in Fig. 1, MD1-MD5 are diode connected MOS transistors, V_{in} is the input supply voltage to the CP, which also acts as the supply voltage of clock generation circuits (not shown in the figure). Clk1 and Clk2 are fully differential non-overlapping clock signals. When Clk1 is low, node 1 is initially charged to $V_{in} - V_{th}$ (where V_{th} is the threshold voltage of NMOS transistor), and when Clk1 is high, node 1 is boosted by an amount ΔV. ΔV can be expressed as [7]

$$\Delta V = \left(\frac{C}{C + C_s} . V_{in} - \frac{I_L}{(C + C_s). f} \right) \tag{1}$$

Where $V_{Clk} = V_{in}$, C is the pumping capacitance which is equal in size (C1=C2=C3=C4=C), C_s is the parasitic capacitance associated with each pumping node, f is the frequency of clock signals, and I_L is the output load current. As all the transistors and capacitors of the CP are equal in size, so the boosted voltage at each node is equal to the ΔV (except output node 5). Voltage is boosted at each stage of CP, hence the voltage gain, Av of each stage of the CP is given by the voltage difference between two consecutive nodes of CP which can be expressed as

$$\mathrm{A}v = V_N - V_{N-1} \tag{2}$$

Where V_N and V_{N-1} are the consecutive node voltages of the CP. Solving Eq. (2), Av can be written as

$$Av = \left(\frac{C}{C + C_s} . V_{in} - \frac{I_L}{(C + C_s). f} \right) - V_{th} \;=\; \Delta V - V_{th} \tag{3}$$

As shown in Eq. (3) for positive voltage gain, ΔV should be greater than the threshold voltage of MOS transistor (V_{th}). Output voltage (V_{out}) of CP is given as

$$V_{out} = V_{in} + N . Av - V_{th} \tag{4}$$

Or one can write equation (4) as [8]

$$V_{out} = V_{in} + N.\left(\frac{C}{C + C_s}.V_{in} - \frac{I_L}{(C + C_s).f}\right) - (N + 1)V_{th} \quad (5)$$

As shown in Eq. (5) voltage drop occurs at each stage of the CP due to threshold voltage of MOS transistor, it becomes critical in application where the input supply voltage is low (in the range of threshold voltage of MOS transistor). Hence, the effect of threshold voltage drop at the output voltage of CP is main drawback of Dickson CP.

To reduce the effect of threshold voltage of MOS transistor or to increase the pumping gain of the CP, many circuits have been reported [7 - 9]. Static Charge transfer switch (CTS) based CP is proposed [7, 8], that uses auxiliary MOS switch chain along with diode connected MOS transistor chain of Dickson CP. These auxiliary MOS switches connected with each stage are driven by higher voltage generated from next stage of the CP to eliminate the effect of threshold voltage in the main switch chain [7, 8]. If the auxiliary MOS switches can be turned ON and OFF at the designated clock period, they can allow the charge to be pushed only in forward direction without any voltage drop and Eq. (5) can be written as

$$V_{out} = V_{in} + N.\left(\frac{C}{C + C_s}.V_{in} - \frac{I_L}{(C + C_s).f}\right) - V_{th} \quad (6)$$

But unfortunately, the auxiliary MOS switch cannot be turned OFF completely in the designated clock period, because the gate voltage of the auxiliary switch during the OFF period of switch is high enough to keep the switch turned ON [7, 8]. The auxiliary MOS switches are always ON and the charge flow in both forward as well as backward direction. The flow of charge in backward direction is called reverse charge sharing. Due to reverse charge sharing effect the voltage fluctuation at each pumping node are different and smaller than the predicted one. As a result, the overall voltage pumping gain of this topology is reduced. To overcome this drawback a dynamic Charge Transfer switch based CP is proposed [7], that provide dynamic control to each charge transfer switch so that it can be turned ON and OFF completely during designated clock period.

Simulated results of dynamic CTS CP match with the theoretical value. But as shown in Eq. (6) pumping gain is limited by the threshold voltage drop at the output stage of the CP, which degrade the output voltage of the CP by the threshold voltage of the MOS transistor, and this voltage drop at the consecutive nodes is increased due to body effect [10].

In both topologies discussed above CTS cannot be used at output stage of CP because there is no required signal present to control the switch. Various techniques have been proposed to reduce the effect of V_{th} such as bootstrapping the clock signal [7], auxiliary MOS based charge transfer block using floating well [9]. However, these techniques increase the complexity or requires additional masks for fabrication which would further increase the cost. This paper proposes an improved dynamic charge transfer switch based charge pump architecture that provides higher pumping efficiency in a standard CMOS process technology.

2 Proposed Charge Pump

2.1 Circuit Description

Fig. 2 shows the schematic diagram of the proposed charge pump circuit based on dynamic CTS with auxiliary PMOS transistor at the output stage. In this schematic, MD1-MD5 (MDs) are diode connected NMOS transistors, MS1-MS4 (MSs) are charge transfer switches (CTS). MS1-MS4 and MD-MD4 connected in parallel to each other. Pass transistors MN1-MN4 (MNs) and MP1-MP4 (MPs) are used to dynamically control of the CTS, so that MSs can be turned ON and OFF completely to remove reverse charge sharing. Clock signals Clk1 and Clk2 are kept out-of-phase with same amplitude (V_{in}) to bootstrap the charge at each node (1-5).

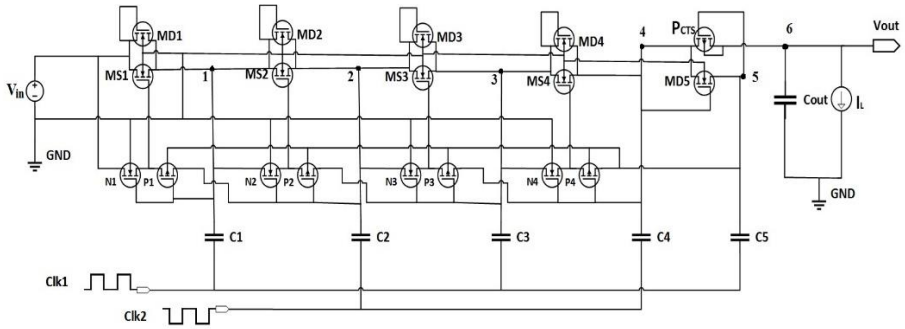

Fig. 2. Schematic diagram of four stage proposed charge pump.

2.2 Operation of the Circuit

Initially, all the pumping capacitors are at zero potential. Under this condition when input voltage is applied, the proposed charge pump circuit acts as Dickson charge pump. The MSs acts as diode connected MOS transistors, this condition is prevailed until the voltages at the nodes reaches the threshold voltage of the NMOS transistor.

After establishing voltage greater than the threshold voltage of NMOS at each node, MSs transistors start working as switches and allow the charge to transfer from one node to another without any voltage drop. Under this condition, when Clk1 goes low and Clk2 goes high the diode MD1 turned ON, but the voltage at node 2 is greater than node 1. MP1 conduct and the gate of MS1 is connected to node 2. Therefore, MS1 switch turns ON and capacitor C1 is charged to input voltage V_{in}. Voltage at node 1 becomes equal to the input voltage V_{in} and therefore MN1 is turned OFF. In the next clock half cycle, Clk1 goes high and Clk2 goes low, MD1 is turned OFF. The voltage at node 2 becomes equal to the voltage at node 1 therefore, MP1 turned OFF. But the voltage at node 1 is greater than V_{in} therefore, MN1 conducts and the gate of MS1 is connected to V_{in} which makes MS1 to turn OFF completely. As shown in Fig. 2 gate of PMOS switch which acts as an auxiliary transistor is connected to node 5. Voltage at node 5 is boosted by Clk1 and voltage at node 4 is boosted by Clk2. When Clk2 is high and Clk1 is low then

the voltage at node 4 is higher than the node 5. Hence, gate-to-source $|V_{gs}|$ voltage become greater than the threshold voltage of PMOS $|V_{thp}|$ transistor, PMOS transistor conduct and voltage at node 4 is transferred to node 6 without any voltage drop. In the next clock half cycle, when Clk2 is low and Clk1 is high, then the voltage at node 5 is higher than the voltage at node 4. Hence, $|V_{gs}|$ become less than the $|V_{thp}|$ which turn OFF the PMOS transistor and higher voltage of node 4 remain stored in output capacitor. By using this technique, the voltage drop at the output of charge pump is removed as compared to an NMOS transistor at the output state [7]. Hence, output voltage of proposed charge-pump circuit is given as

$$V_{out} = V_{in} + N.\left(\frac{C}{C + C_s}.V_{in} - \frac{I_L}{(C + C_s).f}\right) \tag{7}$$

Or if parasitic effect is neglected then the output voltage (V_{out}) can be written as [11]

$$V_{out} = (N + 1)V_{in} - N\frac{I_L}{C.f} \tag{8}$$

As shown in Fig. 2, the output capacitor is charged and discharged periodically which causes ripple in the output voltage of the CP. Amplitude (V_R) of these ripple is given as [8, 11]

$$V_R = \frac{I_L}{f.\ C_{out}} \tag{9}$$

Ripple voltage can be reduced either by increasing the frequency of the clock or by using a large output capacitance. Using large capacitor at the output stage increases the time to reach steady state and also increases silicon chip area.

3 Simulation Results

Four-stage proposed CP based on dynamic CTS CP circuit with pumping capacitance of 50 pF, clock frequency of 20 MHz is designed and simulated in Cadence environment using UMC 0.18 µm CMOS technology.

3.1 Circuit performance

Fig. 3 shows the simulated output voltage of proposed CP circuit with varying load current at different input supply voltages. As load current increases the output voltage of CP decreases linearly as shown in Eq. (7). Fig. 4 shows the difference between simulated output voltage and theoretical value (assuming parasitic capacitor (Cs) = 0) of output voltage at varying input supply voltage and constant load current (50 µA). Maximum difference between simulated and theoretical output voltage of proposed CP circuit is 54 mV at input voltage 0.8 V. This shows that the proposed simple technique is highly efficient. Proposed CP provide output voltage variation less than 10 mV across process corner and less than 8 mV with temperature change from -40˚C to 100˚C.

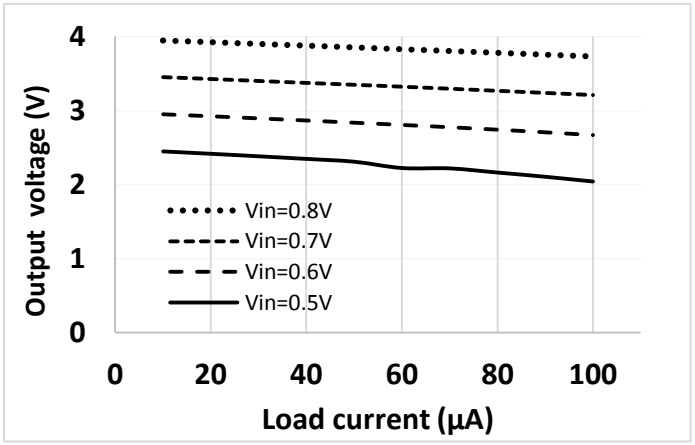

Fig. 3. Simulated output voltage of the proposed CP with varying load at different input voltage.

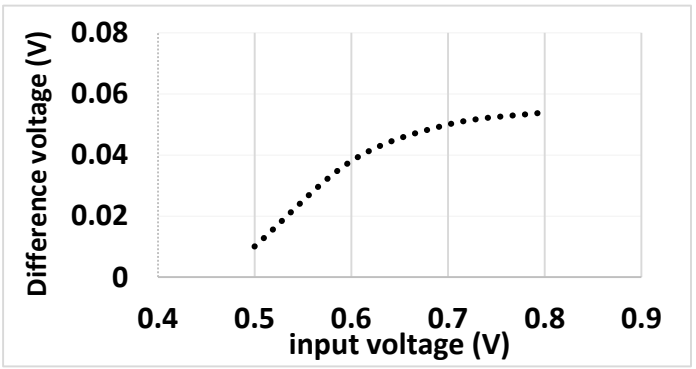

Fig. 4. Difference between theoretical and simulated Output voltage of proposed CP with varyingt input voltage.

3.2 Architecture Comparison

Fig. 5 and Fig. 6 shows the comparison of simulated output voltage for different CP topologies and percentage loss in the output voltage at different input voltages respectively. For reasonable comparison size and values of all MOS switches, capacitors, clock frequency and load current are kept similar. Fig. 5 shows that the output voltage of proposed CP is highest compared to the other topologies. Fig. 6 shows that the voltage loss in output voltage is minimum in the proposed CP circuit.

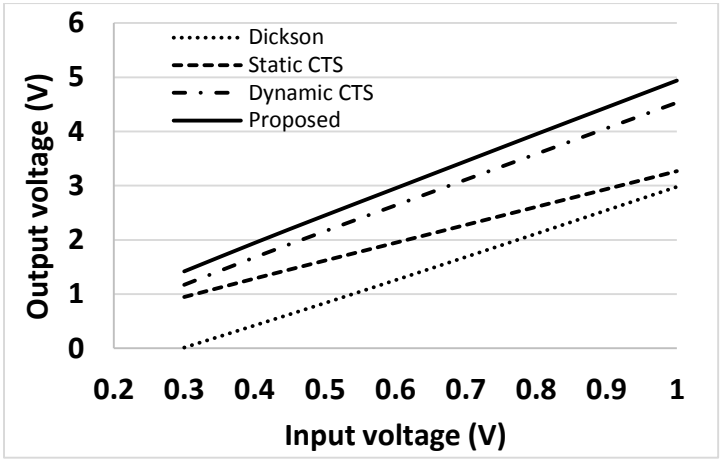

Fig. 5. Comparison of different CP topologies with varying input voltage.

As compared to conventional dynamic CTS based architecture, the proposed circuit reduced the voltage loss at the output to 1.3% as compared to 9% for 1 V input and 6% as compared to 20% for 0.3 V input voltage. And reduced the voltage loss from 99% to 6% for 0.3 V input and from 40.5% to 1.3% for 1 V input voltage compared to the Dickson CP.

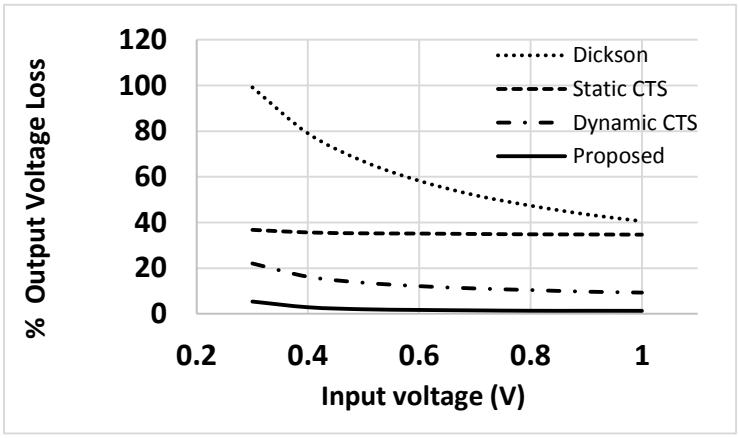

Fig. 6. Percentage loss in output voltage of different CP topologies with varying input voltage.

3.3 Post Layout simulation results

Fig. 7 shows the layout diagram of the proposed CP circuit. The core dimensions of the layout are 750 µm × 530 µm, where 96% of this area is occupied by the capacitors.

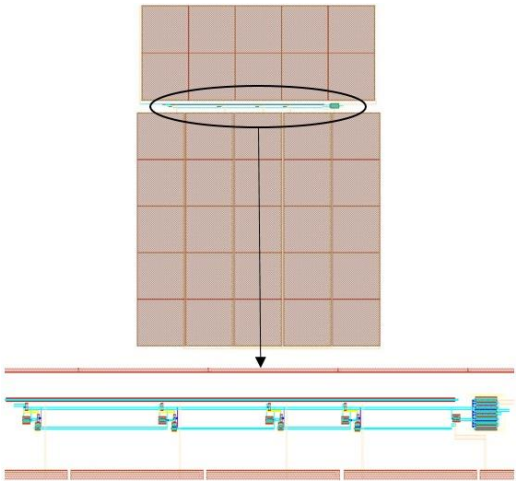

Fig. 7. Layout diagram of proposed CP.

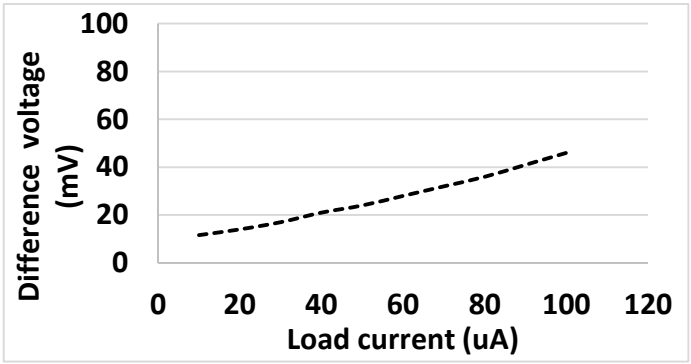

Fig. 8. Difference between Pre-layout and Post-layout output voltage of proposed CP with different load current.

Fig. 8 shows the voltage difference between pre-layout and post-layout simulation results of CP circuit with varying load currents and constant input voltage (0.6 V). As shown in Fig. 8 maximum voltage difference between pre-layout and post-layout simulation results is 46 mV at load current 100 µA. This is basically due to the parasitic resistances and capacitances formed at each node of CP.

Table 1 shows the performance summary of the proposed CP and also, shows the comparison with previous work. By comparing the post-layout simulation results given in the references as shown in Table 1, the technique proposed in this work has higher boosting efficiency at lower input voltage and can deliver more load current above 0.5V input voltage. Also, Proposed CP has 4.6 times higher voltage compared to the Dickson

CP at 400 mV input which is higher than the architecture proposed by [12] that has 3.12 times higher voltage compare to Dickson CP at 380 mV. The chip is ready for fabrication.

Table 1. Performance summary and comparison of charge pumps

	[2]	[3]	[4]	[9]	[12]	This work
Process	TSMC 0.35 µm	0.18 µm	TSMC 0.18 µm	UMC 0.18 µm	65 nm	UMC 0.18 µm
Min. input voltage	3.3 V	1.8 V	0.45 V ~0.55 V	500 mV	290 mV	300 mV
Output voltage	17.5 V	5.62 V	1.26 V	2 V	1.285 V @Vin=0.5 V	1.42 V @ Vin = 0.3V
Output current	5-6 µA	-	310 µA	50 µA @ Vin = 1.4 V	-	100 µA @ Vin > 0.5V
Boosting efficiency	41%	62%	84%	80%	86% @ Vin= 0.5 V	94.67% @ Vin= 0.3 V 98% @ Vin > 0.45 V
Chip area	-	-	850µm × 850µm	-	3000 µm^2	750µm × 530µm

4 Conclusion

A dynamic CTS based highly efficient CP has been designed. Maximum achievable pumping efficiency is 94.67% for input voltage of 0.3 V and 98% for input voltage greater than 0.45 V. Proposed CP is capable to boost the input supply voltage as low as 0.3 V and can deliver a load current up-to 100 µA for input voltage greater than 0.5 V and 40 µA for input voltage less than 0.5 V.

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