Fabrication and Characterization of Al gate n-MOSFET, On-chip Fabricated with Si_3N_4 ISFET

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***Abstract*— This paper reports the fabrication of n-type MOSFET using Si_3N_4 as dielectric on the same chip as ISFET for ISFET characterization. The paper presents the fabrication, simulation and characterization of metal-oxide field-effect transistor (MOSFET). The gate of the ISFET is stacked with Si_3N_4 sensing membrane layer that has been deposited using LPCVD system to cover the gate area. Output and transfer characteristics of on-chip fabricated MOSFET are obtained and measured in order to study the fabricated ISFET behavior to be used as pH sensor. Silicon nitride is preferred over silicon dioxide sensing film/dielectric (in case of MOSFET) which has better sensitivity and low drift. Process simulations were performed using Silvaco® TCAD tool.**

***Keywords*— MOSFET, ISFET, Si_3N_4, Silvaco®**

I. INTRODUCTION

The metal-oxide semiconductor field-effect transistor (MOSFET) is a four-terminal device. In addition to the drain, gate and source, there is a substrate, or body contact. Generally, for practical applications, the substrate is connected to the source terminal. The depletion n-MOSFET device is formed from a p-type substrate with physically implanted/thermally diffused n-type source, drain regions. The dielectric material covers the area between the source and drain to provide electrical isolation.

The ISFET is a derivative of MOSFET that is used to measure the ionic concentration in an analyte. The idea of gating the channel of an FET using the electrostatic interaction between charged molecules adsorbed on the surface of the channel was introduced in the 1970s by Bergveld [1-2]. ISFET consists of a silicon semiconductor substrate with two electrical contacts (source and drain) at a small distance apart. Overlaying the substrate between the source and drain, there is no gate electrode and the insulator is in direct contact with the solution and reference electrode [3].

Silicon nitride is used as the sensing film of the ISFET because the film material is commonly used, available and compatible with standard MOSFET process [4]. With the selection of an appropriate insulator material, such as silicon nitride, hydrogen ions will reside at the surface of the insulator in proportion to the pH. The interaction of insulating material with the ions in the electrolyte results in change in threshold voltage. This leads to a change in conductivity of underlying channel and current flow [5]. A good pH sensitive insulator must possesses linear response over wide pH range, must show high selectivity to H^+ ions and less selectivity to other ions. It must have high sensitivity to concentration changes and must exhibit low drift performance [6].

In this work, the equivalent MOSFET structure has been simulated in Silvaco® containing silicon nitride as dielectric. The MOSFET structure is simulated because it is not possible to simulate the ISFET structure directly in Silvaco® tool. To prove the concept, MOSFET structure was simulated. MOSFET devices are fabricated on the same wafer with ISFET devices to evaluate the electrical performance of the ISFET devices before packaging.

Process and device simulations of the MOSFET are performed using Silvaco®. Characterization of the fabricated devices was performed on KITE-SCS4200. The paper is organized as follows: Section II presents the comparison between ISFET and MOSFET structure. In section III, the simulation, fabrication and device testing are described in detail. Section IV presents results and discussion and the conclusions are drawn in section V.

II. ISFET vs. MOSFET

ISFET combines the principle of MOSFET and a glass electrode. ISFET is similar to MOSFET except the gate part [7]. Unlike MOSFET, gate of MOSFET is replaced by a pH sensing membrane. The sensing membrane is used to detect ion response in the solution by exposing the membrane layer to the solution [8-9]. The gate of a MOSFET consists of a metallic layer and is used as an electrode to control the drain-source current through the external potential V_{gs}. In the case of ISFET, the metallic gate is replaced by a sensing film that is sensitive to hydrogen ion concentration. When immersed in a liquid, the electrical circuit is closed with V_{gs} applied through the reference electrode, and the hydrogen ion concentration in solution can influence the drain-source current [10].

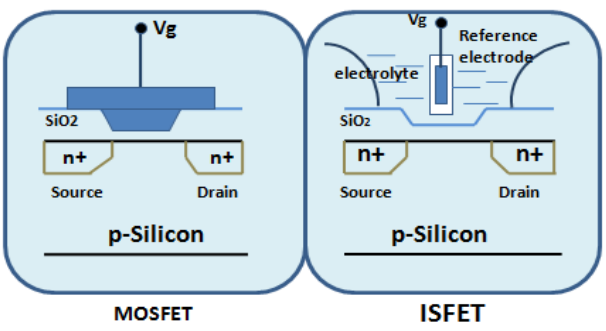

Fig. 1. MOSFET and ISFET structure

III. SIMULATION AND FABRICATION

A. Process Simulation

Athena™ simulator provides general capabilities for physically-based, two-dimensional simulation of semiconductor processing. Athena™ environment was used to simulate MOSFET. Silicon wafer with orientation <100> was used. Firstly, the field oxide of 1 µm thickness was grown over the wafer surface. Then pattering was done to define the source and drain regions. In the diffusion process, doping of phosphorous was done for source and drain regions, followed by drive-in process. Growth of gate oxide and deposition of silicon nitride as a sensing layer with a thickness of 0.05 µm and 0.08 µm was achieved. Then patterning of gate oxide and silicon nitride was done for gate region. For electrical contacts, sputtering of aluminum metal was done. Figs. 2, 3, and 4 show the complete device structure, structure with doping, and doping profile of the source/drain region respectively, as obtained by simulation in Athena™.

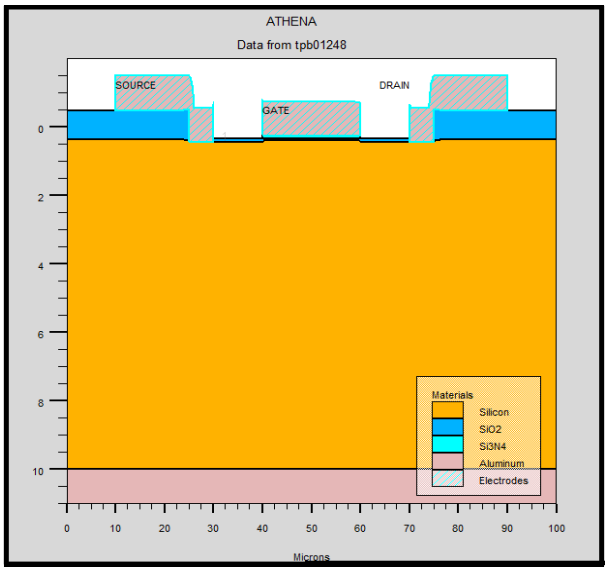

Fig. 2. MOSFET showing various regions/layers

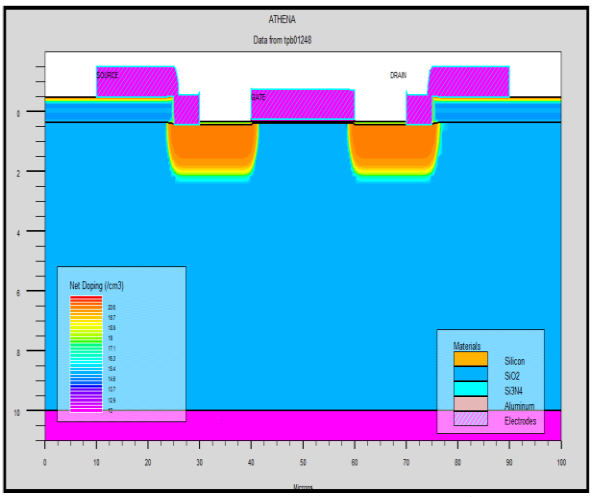

Fig. 3. MOSFET structure with doping profile

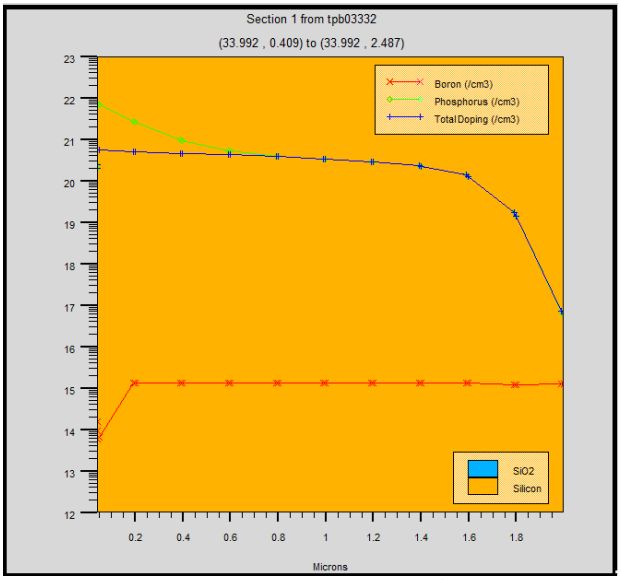

Fig. 4. Doping concentration profile

B. Device Simulation

MOSFET device simulation was performed in Atlas™. Atlas™ provides general capabilities for physically-based two-dimensional (2D) and three-dimensional (3D) simulation of semiconductor devices. The device simulation has been performed to obtain the electrical characteristics. From device simulation, transfer and output characteristics of MOSFET were obtained. For the simulation, Newton method and srh (Schockley Read Hall) model was used.

Transfer characteristics were plotted between drain current (I_{ds}) and gate voltage (V_{gs}), as shown in Fig. 5.

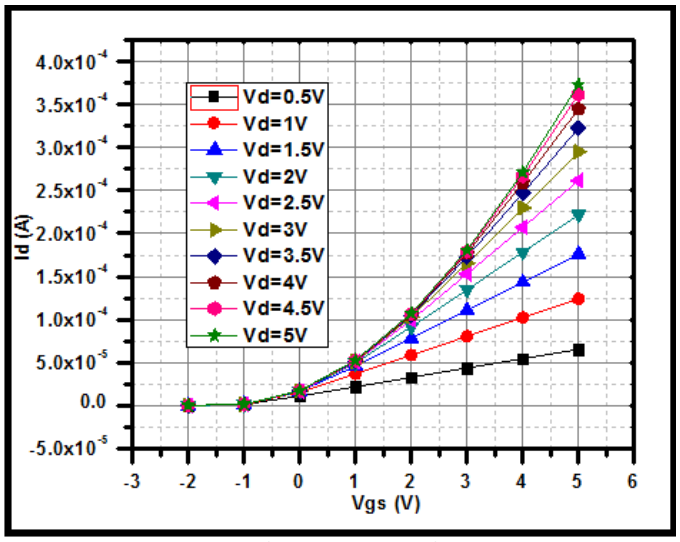

Fig. 5. Transfer characteristics of MOSFET

Output characteristics were plotted between drain current (I_d) and drain-to-source voltage (V_{ds}), as shown in Fig. 6. At the drain terminal, voltage is varied from 0 to 5 V, while gate was biased at different voltages ranging from -2 V to 5 V with the step of 1 V.

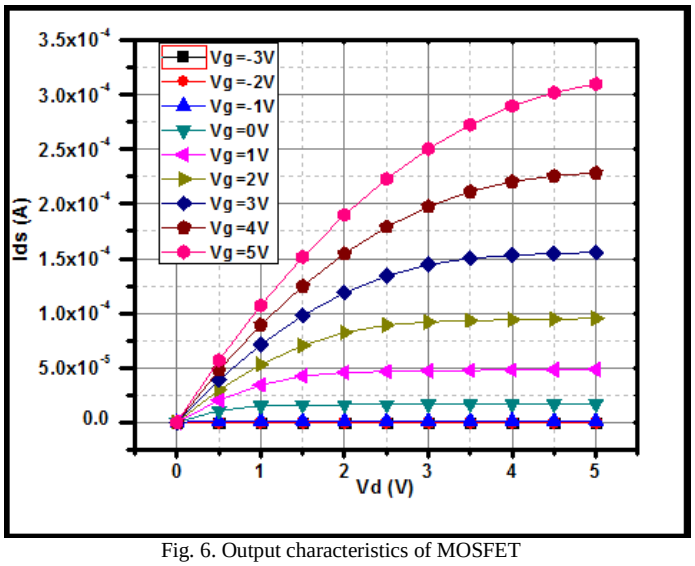

Fig. 6. Output characteristics of MOSFET

C. *Fabrication*

A P-type silicon wafer with resistivity 10 ohm-cm, and orientation <100> was used. Then oxidation was done sequencing dry-wet-dry for 20 min, 120 min, 20 min, respectively at a temperature of 1050°C. A field oxide of thickness 0.854 µm was grown. This was followed by patterning of front side oxide for the source and drain regions using photolithography. The gate oxide of thickness 0.05 µm was grown at a temperature of 1000 °C for 30 minutes. The silicon nitride was deposited using LPCVD (low vapor chemical deposition) at a temperature of 800°C for 23 minutes. Ammonia (80 sccm) and Dichlorosilane (20 sccm) in vacuum of 270 mtorr were used for the deposition of nitride. The thickness of silicon nitride achieved was 0.08 µm. Then silicon nitride and silicon dioxide were etched. To obtain source and drain regions, N-type phosphorous doping (diffusion) was done at a temperature of 1050°C for 30 minutes followed by drive-in process at a temperature of 1050 °C for 30 minutes. A sheet resistance of 1.88 Ω/square and junction depth of 1.72 µm were achieved. Aluminum was sputtered on front and back sides of the wafer by RF sputtering, followed by photolithography for patterning of Al metal. Finally, from the front side of the wafer, Al was etched using commercial Al etchant.

D. *Device Testing*

For the *I-V* characterization of MOSFET, Keithley Interactive Test Environment SCS-4200 system, was used in conjunction with Cascade Microtech (MPS150) DC probes. The 4200-SCS is a modular, fully integrated parameter analyzer that performs electrical characterization of materials, semiconductor devices and processes. *I-V* characterization test setup is shown in Fig. 7. The three probes were connected to gate, source and drain, respectively and the bulk was kept at ground. A voltage sweep at drain terminal was provided with the step of 0.5 V and voltage sweep at gate terminal was provided with the step of 1 V. The corresponding current through the MOSFET was measured.

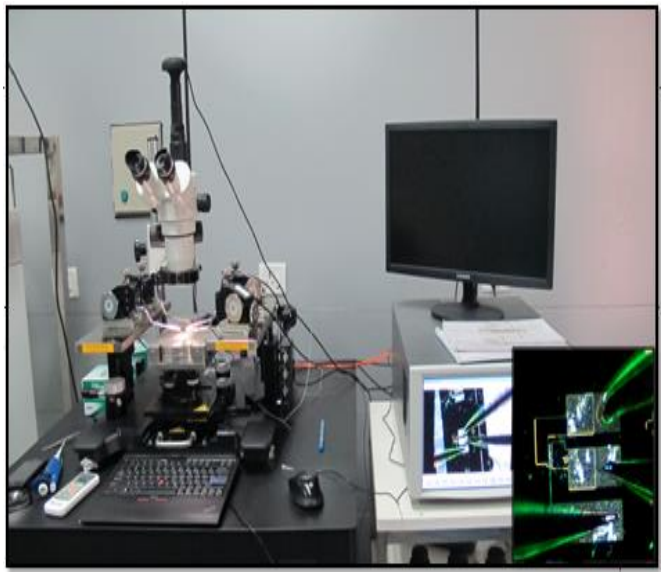
Fig. 7. Testing setup

The graph of drain current I_d vs. gate voltage V_{gs} with a constant drain voltage for MOSFET is shown in Fig. 8. At gate terminal, voltage sweep from -2 to 5 V was provided while drain was biased at different voltages ranging from 1 V to 5 V with the step of 0.5 V. It can be seen from the plot that drain current increases as V_{ds} increases.

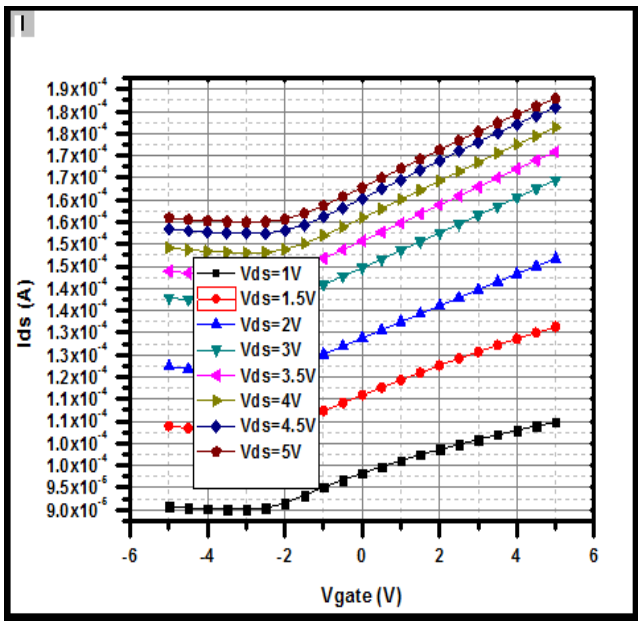

Fig. 8. *I-V* characterization (I_{ds} vs. V_{gs})

The drain current vs. drain voltage V_{ds}, at a constant gate voltage is shown in Fig. 9. At the drain terminal, voltage sweep from 1 to 5 V was provided while gate was biased at different voltages ranging from 1 V to 5 V with the step of 1 V. From the plot it has been observed that as gate voltage increases from 1 to 5 V, drain current also increases.

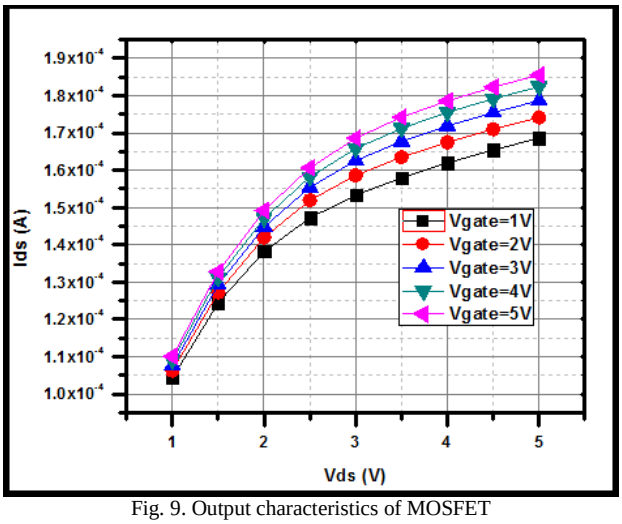

Fig. 9. Output characteristics of MOSFET

IV. RESULTS AND DISCUSSION

The thickness of field oxide was found 0.854 µm. Silicon nitride was deposited using LPCVD because of high strength over wide range of temperatures. Sheet resistance of N^+ layer was found to be 1.88 Ω/square. From the output and transfer characteristics, it is clear that MOSFET is working in depletion mode. The threshold voltage is ~ -2 V, which is in agreement with the simulated results in which the device is also working in depletion mode, i.e., the threshold voltage is -1 V. The deviation in the threshold voltage is due to the fabrication imperfections and interface trapped charges.

Silicon nitride is chemically reactive and has low drift with temperature. Also as a sensing film, it is compatible with MOSFET device fabrication. As a sensing film, SiO_2 has shortcomings like low sensitivity to pH, higher drift and hydration problems. To overcome all these shortcomings, silicon nitride was used in present device fabrication and simulation.

V. CONCLUSIONS

Fabrication and simulation of MOSFET have been presented. Silicon nitride was used as a sensing film (dielectric in case of MOSFET) for the better performance of the device as pH sensor. Process simulation was carried out in Athena™ and device simulation was performed in Atlas™. *I-V* characterization was carried out in Keithley Interactive Test Environment SCS-4200 system.

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