Simulation and Characterization of Dual-Gate SOI MOSFET, On-chip Fabricated with ISFET

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***Abstract*— The paper presents the process design, simulation and characterization of a silicon-on-insulator (SOI)-based dual-gate metal oxide field-effect transistor (DG MOSFET) with Al metal gate. The proposed structure is an N-channel device, using aluminum nitride (AlN) as gate dielectric. The fully depleted SOI-based DG ISFET compatible with the complementary metal-oxide-semiconductor (CMOS) process is considered to be a very promising bio-chemical sensor. Process design and simulations are performed by using Silvaco® TCAD tool. The simulated and experimental results are compared, and are found to be in good agreement.**

***Keywords* — Dual-gate SOI MOSFET, Aluminum Nitride (AlN), ISFET**

I. INTRODUCTION

SOI-based devices have shown their potential for many applications, such as high speed CMOS circuits, three-dimensional circuits, and sophisticated solid state sensors. SOI transistor is a thin film device having four terminals. These are source, drain, front gate and backside gate. The physics of SOI MOSFET is highly dependent on the thickness of the silicon film and its doping concentration in which the device is fabricated [1]. There are two main types of standard SOI-MOSFET devices, fully depleted and partially depleted, distinguished on the basis of depletion in the channel region. In partially depleted SOI (PDSOI) device, the silicon film thickness is greater than maximum depletion width, whereas in a full depleted SOI (FDSOI) device, the silicon film thickness is less than the maximum depletion width. In the latter case, the silicon film is fully depleted at threshold, irrespective of the bias applied to the back gate. FD SOI MOSFET with depleted back interface exhibits the most attractive properties such as high transconductance, low electric field, excellent short-channel behavior, and better sub-threshold slope characteristics [2-4]. In the FDSOI-MOSFET, the depletion zone is controlled by the front-gate potential via the gate-oxide (C_{ox}) and buried oxide capacitances (C_{box}), respectively [5].

Silvaco® TCAD tool is used to simulate the MOSFET test structure with aluminum nitride as sensing layer, because the ISFET structure cannot be simulated directly in Silvaco simulation tool. The structure of ISFET is based on metal oxide semiconductor field effect transistor, in which the metal gate electrode is replaced by an electrolyte solution with a reference electrode (Ag/AgCl) [6-7]. SOI ISFET is ion-sensitive field-effect transistor, which is used for measuring ionic concentration of an analyte. When the ionic concentration changes the current through the transistor will change accordingly, due to change in interfacial potential.

ISFET was first proposed by Bergveld in 1970s. ISFET technology has various applications in environmental, chemical and biomedical fields such as blood monitoring, environment monitoring, biological analysis, chemical analysis and clinical detection [8]. ISFET has many advantages of exploiting mature semiconductor technologies such as small size, simple structure, easy integration, label free detection and high compatibility with complementary metal oxide semiconductor transistor technology [9-10].

Dual-gate (DG) operation of the MOS structure is simulated in order to increase the transconductance of the designed structure. This DG operation amplifies the sensitivity of final ISFET structure, without additional amplification circuits by inducing capacitive coupling between the top and the bottom gate oxide of the SOI wafer [11]. Especially, in biological sensing application, DG ISFET has tremendous potential because it can greatly enhance the small signal monitored during biological events such as nucleic acid hybridization, protein protein interactions, enzyme substrate reaction and antigen antibody binding [12].

The following section presents the process design and simulation of SOI-based DG MOSFET. The fabrication of device structure is discussed in section 3. The experimental results and discussion are reported in section 4, followed by the conclusions.

II. SIMULATION

A. Process simulation

MOSFET process simulations are carried out in Athena™. Athena is Silvaco's virtual wafer fabrication (VWF) process simulator, used for device fabrication. Atlas and Deckbuild simplify the device to a more basic level while Athena™ uses designs realized from actual industrial fabrication [13]. Athena incorporates almost all the fabrication processes used in IC design into a single framework.

The process steps fed into Athena™ for fabricating MOSFET are as follows: SOI wafer is used for complete dual gate operation MOSFET. The device layer, buried oxide and handle wafer thickness of SOI wafer are 1 µm, 1 µm and 400 µm, respectively. The first step is to grow a field oxide layer of thickness 1.0 µm and pattern it to define the source and drain regions. In the diffusion process, doping with phosphorous is done with concentration of 1.0E22 cm^{-3} to form the source and drain regions, followed by drive-in process. After diffusion process, gate oxide is grown and aluminum nitride is deposited, which acts as a sensing layer, with a thickness of 0.05 µm and 0.1 µm, respectively. After deposition, gate oxide and sensing layer AlN are patterned for the gate region. Finally, metallization is done using sputtering of

aluminum metal, for taking electrical contacts of the device.

Figs. 1, 2 show the complete device and doping profile of the structure.

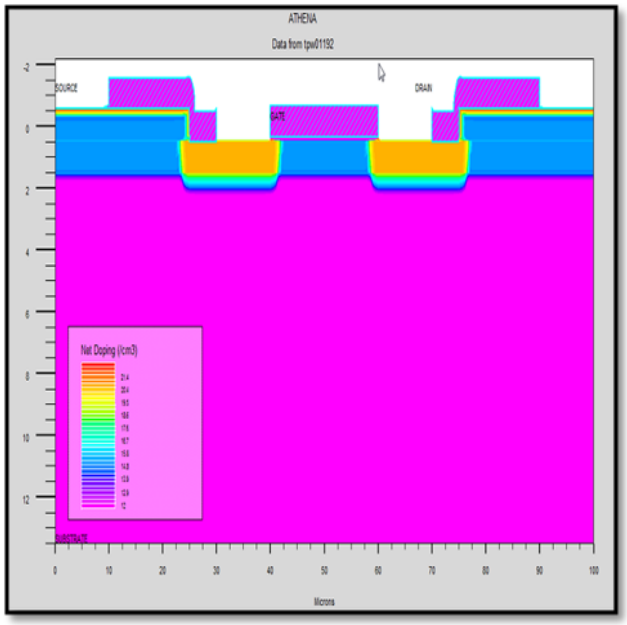


Fig. 1. Device structure of dual-gate AlN MOSFET

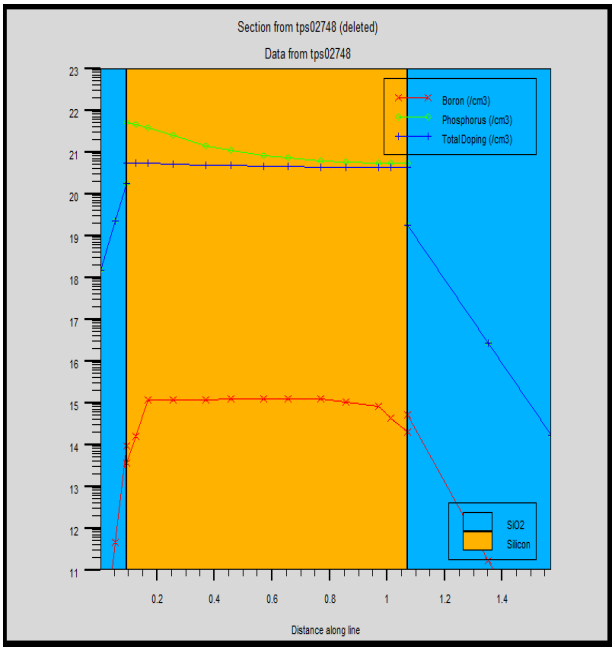


Fig. 2. Source and drain doping profile

B. Device Simulation

MOSFET device simulations are done in Atlas™. Device simulations were carried out using Newton method and Shockley-Read-Hall recombination model with fixed carrier lifetime (SRH). From device simulation, transfer and output characteristics of N-channel MOSFET are obtained at 300 K [13].

Transfer characteristics are drawn between drain current (I_{ds}) and gate voltage (V_{gs}) which is varied from -5 to 5 V with constant drain voltage V_{ds} (1V) for SOI MOSFET, as shown in Fig. 3.

The threshold voltage of the device reduces as the back gate voltage is increased. The threshold voltage of an N-channel depletion mode MOSFET device is extracted from the transfer characteristics, and it is found to be -1 V. The maximum drain current obtained from the transfer characteristics is 1.3 mA for a substrate backside voltage V_{sub} (40V).

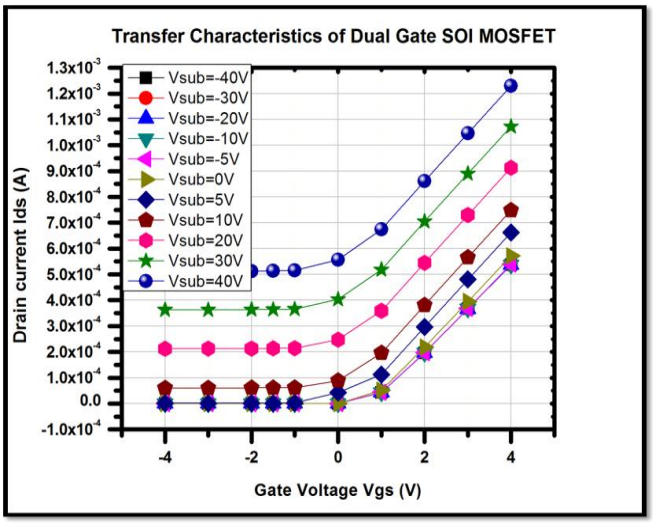


Fig. 3. Transfer characteristics of SOI MOSFET

Output characteristics are drawn between drain current (I_{ds}) and drain-to-source voltage (V_{ds}) with constant back gate voltage, as shown in Fig. 4. As shown in both the output characteristics, drain current increases by increasing front gate voltage and back gate voltage, respectively.

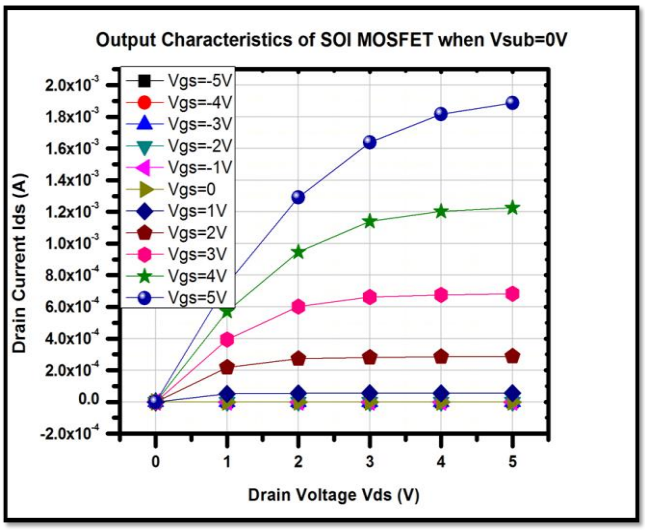


Fig. 4. Top gate output characteristics of SOI MOSFET with V_{sub}=0V

Output characteristics are drawn between drain current (I_d) and drain-to-source voltage (V_{ds}) with constant back

gate voltage. Fig. 5 shows the output characteristics at front gate voltage of 0.5 V (V_{gs}).

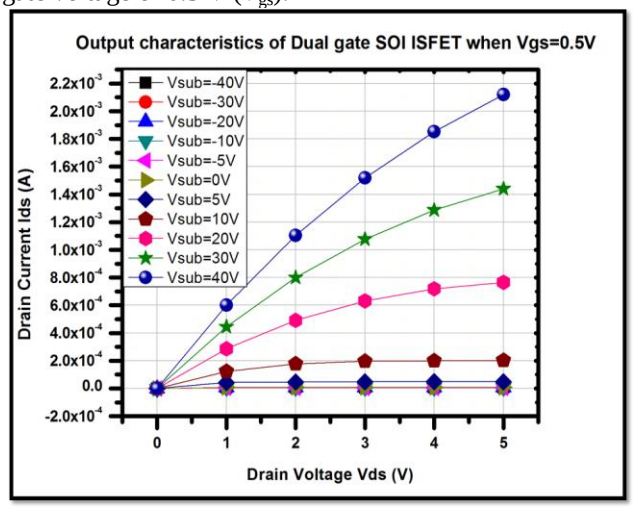


Fig. 5. Back gate output characteristics of SOI MOSFET

III. FABRICATION PROCESS

A P-type <100> silicon-on-insulator wafer with resistivity 10 ohm-cm is used for the process. Initially silicon layer thickness was 2 µm. Thermal oxidation is done, sequencing dry-wet-dry for 20 min, 120 min, 20 min, respectively at a temperature of 1100 °C for thinning of active layer of SOI wafer and a silicon thickness of 1.0 µm thick is achieved. After thinning, the thermal oxidation cycle is repeated to obtain 1.0 µm field oxide over active layer. The final active layer thickness is 1.0 µm .This is followed by patterning of front side oxide for the source and drain regions using photolithography (Mask-1) [14]. After defining source and drain regions, N-type phosphorous doping (diffusion) is done at a temperature of 1050 °C for 30 minutes followed by drive-in process for profile control at a temperature of 1050 °C for 30 minutes. After drive in process, the sheet resistance of active layer is found to be 1.69 Ω/square. The second lithography (Mask-2) is done to define gate region. Then gate oxide is grown at a temperature of 1000 °C for 60 minutes using TCE dry oxidation [15]. Aluminum nitride is deposited as a sensing layer at a temperature of 100°C for 10 minutes using pulsed DC reactive sputtering. Thicknesses of the gate oxide and aluminum nitride sensing layer are 0.05 µm and 0.1 µm, respectively. Following this, lithography for contact window opening is performed using mask 3. Aluminum nitride and silicon oxide layers are etched using aluminum etchant and BHF respectively. Finally, aluminum is sputtered on front and back side of the wafer, followed by photolithography for patterning of Al metal using Mask 4. From the front side of the wafer, Al is etched using commercial Al etchant, keeping the back side coated with photoresist to protect Al on the back side. At last, aluminum sintering is done at 450 °C, which besides improving the metal semiconductor contact also reduces the surface state density at semiconductor/ gate oxide interface [15]. The length (L) of the channel of MOSFET device is 20 µm and width (W) of the channel is 400 µm. The complete process design and fabricated device structure of SOI based DG ISFET and MOSFET are shown in Fig. 6. Fig. 6 (i) shows the cross-sectional view at different process stages, Fig. 6 (ii) the processed "4" inch wafer with ISFET and MOSFET devices and Fig. 6 (iii) the fabricated ISFET and MOSFET chips.

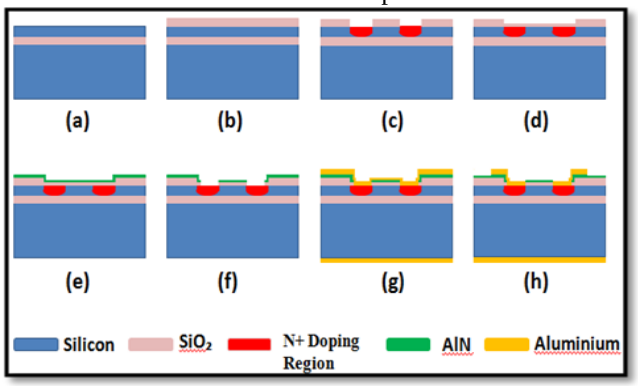


Fig. 6(i)) Fabrication process flow chart of Dual gate ISFET- (a) Starting SOI wafer, (b) Oxidation, (c) Oxide etching, phosphorous diffusion and Drive- in, (d) Gate oxide growth using TCE oxidation, (e) Sensing layer AlN deposition, (f) Etching of gate oxide and sensing layer (AlN), (g) Aluminum deposition and (h) Aluminum pattering.

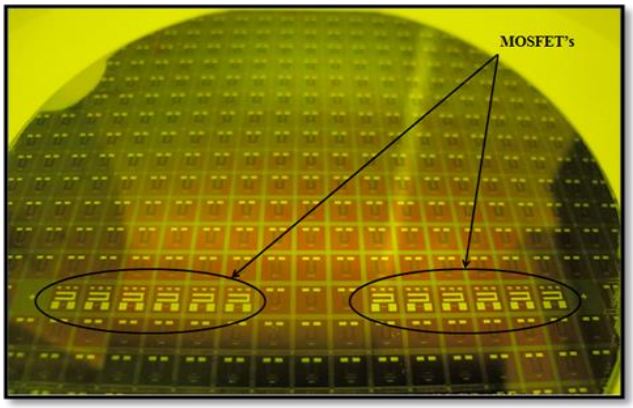
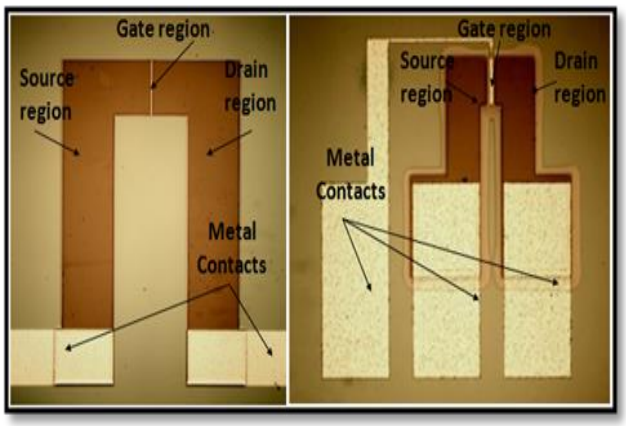


Fig. 6 (ii). Processed 4-inch wafer with fabricated ISFET and MOSFET devices



(a) ISFET (b) MOSFET

Fig. 6 (iii). Fabricated devices of ISFET and MOSFET chips

IV. DEVICE TESTING RESULTS

For the characterization of Dual gate MOSFET, a Keithley Semiconductor characterization system (4200-SCS) is used in conjunction with Cascade Microtech (MPS150) DC probes. Testing setup is shown in Fig. 7. The drain and gate voltages are varied in steps of 1 V each and the corresponding currents through the MOSFET are measured.

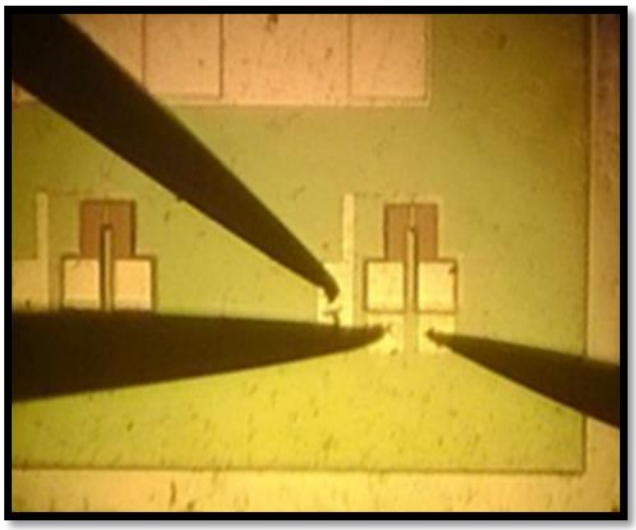


Fig. 7. Testing setup (biasing arrangement)

Fig. 8 shows the measured current in SOI transistor as a function of front gate voltage for different values of backside gate voltage (-40 to 40 V) with constant drain voltage (V_{ds}=1V). The threshold voltage is found to be -2V.

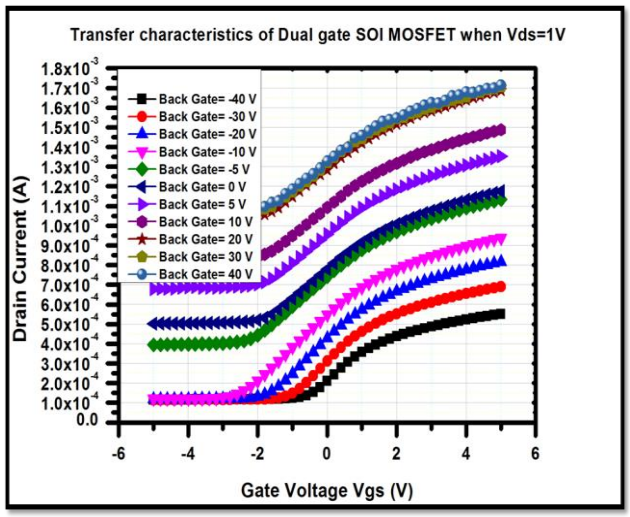


Fig. 8. Transfer characteristics of SOI MOSFET with V_{ds}= 1V

In Fig. 9, current is measured in SOI transistor as a function of drain voltage for different values of front gate voltage (-5 to 5 V) with constant backside substrate voltage. Maximum current obtained is 4.6 mA.

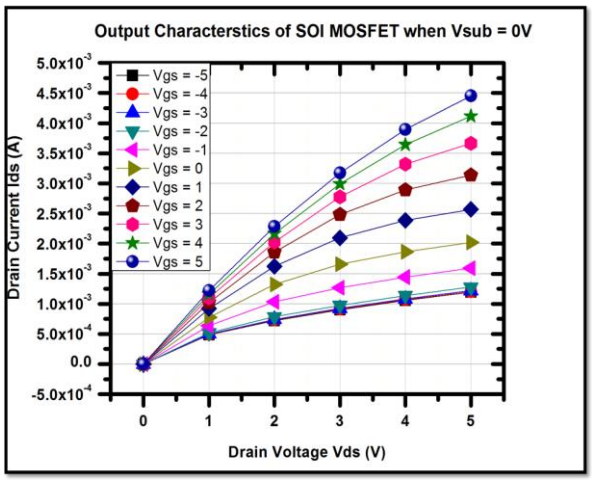


Fig. 9. Output characteristics of SOI MOSFET with V_{sub} = 0V

In Fig. 10, output characteristics are drawn between drain current and drain voltage with constant gate voltage V_{gs} = 0.5 V. Current increases by applying back gate voltage due to formation of channel at the interface of BOX and active layer of silicon.

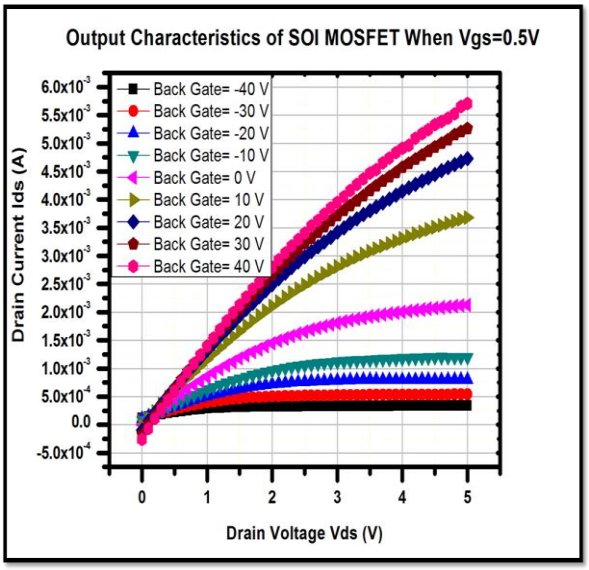


Fig. 10. Output characteristics of SOI MOSFET with V_{gs} = 0.5V

V. RESULTS AND DISCUSSION

Measurement of thickness of field oxide is done by Dektak surface profiler and the thickness is found to be 0.93 µm; the field oxide thickness that is obtained in simulation is 0.851 µm. Gate oxide and aluminum nitride thickness are also found to be in close proximity with the experimental result. Sheet resistance of N^+ layer is found to be 1.69 Ω/square which is close to the simulated result, i.e., 1.64 Ω/square.

The simulated transfer characteristic has a threshold voltage is -1 V, which is in close proximity with the experimental result (-2 V). This shows that MOSFET

conducts when negative gate bias is applied, which indicates that ISFET is an N-channel depletion-mode device. Process-induced unwanted charges might have been trapped in gate oxide, which can change the threshold voltage from -1V to -2 V.

Aluminum nitride is used as sensing film material because of its compatibility with MOSFET device fabrication. Earlier, SiO_2 was used as a sensing film which shows a low sensitivity to pH, exhibits higher drift and it also has hydration problem. To overcome all these issues, aluminum nitride is used as a sensing film.

VI. CONCLUSIONS

Unit process simulation, fabrication and characterization of an N-channel, depletion-mode aluminum nitride gate SOI MOSFET structure have been presented. The simulation and experimental results are found to be closely matching. Aluminum nitride is used as a sensing film for better performance of the ISFET device. Process simulations are carried out in Athena and device simulations are done in Atlas™. Characterization is done using Keithley semiconductor characterization system (4200-SCS).

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REFERENCES

[1] Bergveld, "Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements", IEEE Trans. Biomed. Eng.,Vol. 17, No. 70, 1970.

[2] Li-Chen Yen, Ming-Tsyr Tang, "Effect of Sensing Film Thickness on Sensing Characteristics of Dual-Gate Poly-Si Ion-Sensitive Field-Effect-Transistors", IEEE Electron Device Letters, Vol. 35, No. 12, 2014.

[3] In-Kyu lee, K. Hyi lee, S. lee, Won Ju Cho, " Microwave annealing effect for highly reliable biosensor: Dual–Gate Ion-Sensitive Field – Effect transistor using Amorphous InGaZnO thin- Film Transistor", ACS applied Materials & Interfaces, Vol. 6, pp. 22680-22686, 2014.

[4] Colinge J-P, "Silicon-On-Insulator Technology: Materials to VLSI", Third ed. London: Kluwer academic publishers; 2004.

[5] Jimenez-Jorquera, C., Orozco, J. and Baldi, A., "ISFET based microsensors for environmental monitoring", Sensors 10, pp. 61–83, 2010.

[6] Knopfmacher, O. et al., "Nernst Limit in Dual-Gated Si-Nanowire FET", Sensors Nanolett. 10, pp. 2268–2274, 2010.

[7] Lee, C. S.; Kim, S. K.; Kim, M. "Ion-Sensitive Field-Effect Transistor for Biological Sensing", Sensors, Vol. 9, pp. 7111−7131, 2009.

[8] Spijkman, M.-J. et al., "Dual-Gate Organic Field-Effect Transistors as Potentiometric Sensors in Aqueous Solution", Adv. Funct. Material 20, pp. 898–905, 2009.

[9] Thomas Error, Gerard ghibaudo, T.Ouisse et.al, "Ultimately thin double Gate SOI MoSFETs", IEEE transactions on electron devices, Vol. 50, No. 3, March 2003.

[10] Colinge, J.-P., "Transcoductance of silicon-on-insulator (SOI) MOSFET's", IEEE Electron Device Lett., EDL-6, 573–574, 1985.

[11] Lim, H. K. & Fossum, J. G., "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's", IEEE Trans. Electron Devices 30, pp. 1244–1251, 1983.

[12] Ohata, A., Pertet, J., Cristoloveanu, S. & Zaslavsky, "A Correct biasing rules for virtual DG mode operation in SOI-MOSFETs", IEEE Trans. Electron Devices 52, pp. 124–125, 2005.

[13] Fz. Rahou, A. Guen-Bouazza, M. Rahou, "Electrical characteristics comparison between fully- depleted SOI MOSFET using Silvaco software", Global Journal of Researches in Engineering Electrical and Electronics Engineering", vol. 1, Ver. 1, 2013.

[14] V K Khanna, "Advances in chemical sensors, biosensors and Microsystems based on ion-sensitive-field effect transistor", Indian journal of pure & Applied Physics, Vol. 45, pp. 345-353, 2007.

[15] V K Khanna, "Fabrication of ISFET microsensor by diffusion-based Al gate NMOS process and determination of its pH sensitivity from transfer characteristics", Indian Journal of Pure & Applied Physics, Vol. 50, pp. 199-207, 2012.

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