An Investigation Of Different Stress-free Passivation Layer Designs In GaN HEMTs

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Abstract. Different stress-free silicon nitride passivation layer designs were simulated using simulation software Silvaco. Different SiN_x passivation layer designs (passivation only between the gate-source and gate-drain, passivation edge exactly touching the edges of source and drain contacts and coming over the gate, passivation edges partially covering the source and drain contacts and completely covering the gate, passivation only in the channel area and completely covering the gate) were checked to study their role in GaN HEMTs device improvement process. Resulted Drain current (I_{ds}) was recorded to be the same in all the different designs. A comparatively lower value of transconductance (g_m) was observed in the design having passivation layer exactly touching the edges of source and drain contacts and coming over the gate. Therefore this design was not recommendable. Devices suffered with high gate leakage current independent of design types. An introduction of traps in AlGaN layer surprisingly reduced the gate leakage current in such structures.

Keywords: GaN HEMTs, Gate leakage, traps.
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INTRODUCTION

Surface passivation has proved to be promising in improving the overall performance of GaN HEMTs technology. However a wrong passivation design could adversely affects the device performance. For an example, the over gate passivation often results in an increase of the gate leakage current, which was explained as a consequence of the passivation layer stress experienced by the gate [1].

In this paper we present a detailed simulation work on different stress-free SiN_x passivation layer designs. Different designs including over gate passivation designs were analyzed. An impact on d.c parameters was checked. In particular, Gate leakage current with and without traps was studied.

EXPERIMENTAL RESULT

A basic device of 1x100 µm used for simulation had an AlGaN layer of 25 nm and a GaN buffer of 2.7 µm. Table 1 summarizes different passivation layer designs used for the simulations (covering channel area excluding over gate, block designs including over gate and simple over gate passivation).Output characteristics did not show any difference. Same value of the drain current (0.84 A/mm @ V_{gs} =+2.0 V) was obtained for all the designs.

Fig. 1 shows the resulting g_m. At low voltage, g_m of design A (130 mS/mm) was less in comparison to other designs (170 mS/mm). This decrement was the combined effect of reduced carrier concentration and electric field in this design, which could probably be a consequence of side edge effects. At high voltage, same value of g_m (280 mS/mm) was noticed for all the designs as a result of increased compensated electric field.

TABLE 1. List of designs.

Designs	Descriptions
Standard	Passivation layer only between source-gate and gate-drain.
A	Passivation edge exactly touching the edges of S and D contacts and coming over the gate and channel area. (block design including over gate)
B	Passivation edge partially covering the S and D contacts and completely covering the gate and channel area.(block design including over gate)
C	Passivation layer in the channel area and completely covering the gate. (Simple over gate design)

Fig. 2 shows the leakage current without (a) and with traps (b). All the different passivation designs including or excluding over gate passivation showed a similar value of leakage current (Fig. 2a). On the contrary, reference [1], indicated a high leakage current resulting only from over gate passivation due

to implanted stress by passivation layer over the gate. Since we used stress free nitride, we did not observe any such difference. Therefore the best possible way to reduce the leakage would be a stress free over gate passivation layer.

Next, we introduced traps in the AlGaN layer to check their effect on the device performance in relation to different passivation designs. Used activation energy was 1.12 eV [2].

Irrespective of the passivation design type, a drastic reduction in leakage current was observed as shown in Fig 2 (b).

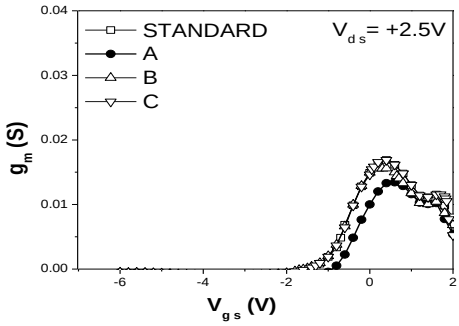
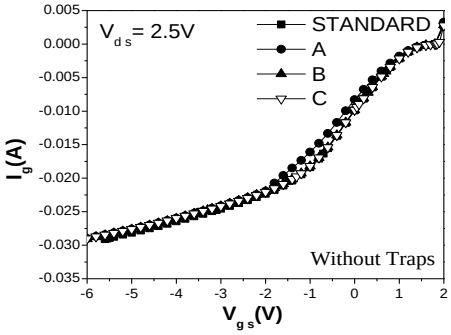
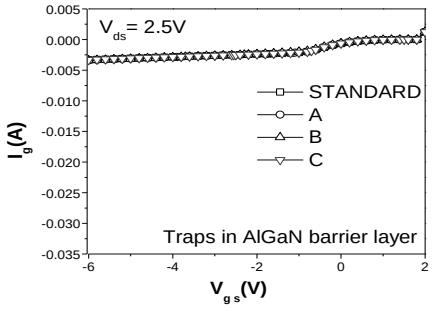


FIGURE 1. Transconductance of different designs



(a)



(b)

FIGURE 2. Leakage current of different designs

Reason behind this strange phenomenon could be very well explained using the carrier distribution shown in Fig. 3. We predicted that after introducing traps in AlGaN layer, tunneling current component (leakage) path was blocked or discontinued under the gate, so leakage current reduced. Also the carrier confinement in case of trapped structure became better due to strong suppression of scattered carriers in the spacer layer.

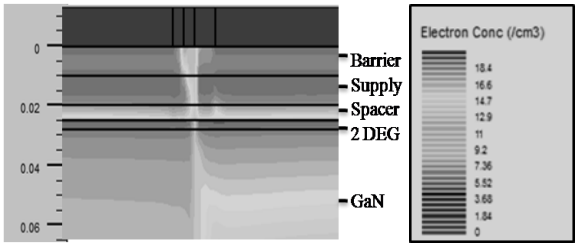


FIGURE 3. Carrier distribution with traps.

CONCLUSION

Different stress-free SiN_x passivation layer designs were simulated. Same value of the I_{ds} was obtained for all the designs. At low voltage, g_m of design A was less in comparison of other designs, this decrement was the combined effect of reduced concentration and electric field. At high voltage, same value of g_m was noticed for all the designs as a result of increased electric field. Different passivation designs including or excluding over gate passivation did not show any difference in the leakage current mainly due to the use of stress free nitride. Surprisingly, irrespective of different passivation designs, an introduction of traps in AlGaN layer drastically reduced the gate leakage current due to blockage of tunneling current component path under the gate.

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