**Category: 'Nanotechnology and Emerging areas'**

# Silicon Nanoparticles for Floating Gate Memory Application

Rahul Prajesh, Sanjeev Kumar and A. Kumar
*CSIR-CEERI Sensors and Nanotechnology Group, Pilani 333031, India*
E-mail: rahulprajesh@gmail.com

***Abstract*—** In this paper we demonstrate memory application of silicon Nano particles. A MOS capacitor with nanoparticles sandwiched between tunneling and capping oxide was fabricated and characterized. Write '1' and write '0' operations are verified by C-V measurements. Flat-band voltage shift in the C-V Curves explains the charge storage behavior of MOS capacitor. Interface charges, flat band and threshold voltages are estimated using Poisson's equation and numerical methods.

***Index Terms* — Nano Particles(NP), Floating Gate Memory, threshold voltage shift, write '1' & write '0' operation.**

## I. INTRODUCTION

From past few years, Nanoparticles are being explored [1-7] extensively because of their applications in Nano electronics [1-4], Bio-sensing [5, 6] and Optics [7]. Nanoparticles have shown new directions to the floating gate memories. Many researchers have attempted with different nanoparticles [1-4] to make floating gate memories. Silicon nanoparticles [3] can also be used to for memory application as these are compatible to CMOS silicon processing. Silicon nanoparticles can be deposited easily with CVD techniques (LPCVD & PECVD). In the presented work MOS capacitor with embedded silicon nanoparticle is fabricated and characterized.

## II. EXPERIMENTAL DETAILS

In this work we started with P type silicon wafer with <100> orientation, Resistivity 1-10 ohm-cm and thickness 275micron. Dry thermal oxide was grown to make a tunneling layer (~2nm) on the wafer. Oxidation was done at 800˚C temp for 2min, with loading and unloading of wafer in nitrogen environment. Then silicon nanoparticles on the tunneling oxide by LPCVD (45sec, 100mTorr, 575˚C, 48.4 sccm) were deposited. We further deposited a capping layer of oxide (~15nm) by PECVD (15sec, 100mTorr, 60watt, 350˚C) on silicon nanoparticles. Then we sputtered Aluminum (1% Silicon) (~0.3micron) on front and back side of the wafer followed by MOS device patterning and 20 min sintering in forming gas environment. FIG.1. shows a schematic of the cross-section of fabricated MOS capacitor structure.

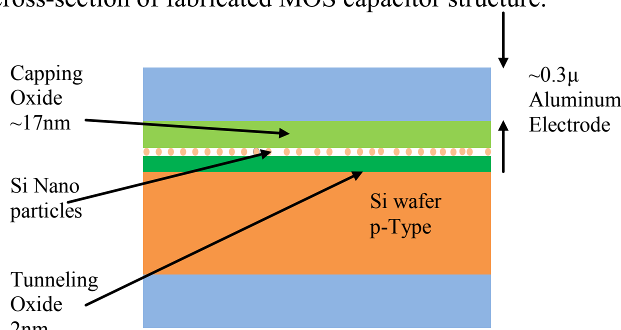


FIG.1. Schematic of MOS capacitor with sandwiched nanoparticles

## III. RESULTS & DISCUSSIONS

C-V curves are plotted to demonstrate the effect of nanoparticles sandwiched in the MOS capacitor. Fig.2 shows the C-V curve of MOSCAP devices with and without nanoparticles. Write '1' and write '0' operations of MOSCAP devices can clearly be seen from C-V curve in FIG.2. MOSCAP with nanoparticles is stresses by ±5V and Flat-band and threshold voltage shift was observed. C-V measurements were done with KEIHTLEY instrument. Further the C-V data was analyzed to extract different parameters from C-V curve. We started with oxide thickness extraction by using accumulation region (C-V w/o NP) capacitance value ($3.77\times10^{-10}$), gate area $1.9635\times10^{-7}$ and permittivity values 3.9 and 4.2 for thermal oxide and PECVD oxide respectively. Oxide thickness values extracted are 2.0nm and 17.2nm for thermal oxide and PECVD oxide respectively. For nanoparticles' height extraction accumulation capacitance value from C-V data for MOSCAP with NP was used and particles' thickness values were verified to be 1.65nm. Flatband voltage was calculated by first calculating $C_{FB}$ (flatband Capacitance) by formula [8]

$$C_{FB} = \frac{C_{ox}\epsilon_s A/(1\times10^{-4})(\lambda)}{(1\times10^{-12})(C_{ox}) + \epsilon_s A/(1\times10^{-4})(\lambda)}$$

Where,
$C_{ox}$=Oxide Capacitance
$\epsilon_s$=Material permittivity
A=Gate Area, and
$\lambda$=Debye length; $\lambda = \left(\frac{\epsilon_s kT}{q^2 N_x}\right)^2$, here kT is thermal energy at room Temperature, q is electron charge, $N_x$=$N_A$
This $C_{FB}$ value corresponds to a voltage in C-V curve that voltage is $V_{FB}$ (flat-band Voltage).
For threshold voltage extraction we used the concept
$\emptyset_s = 2\emptyset_B$ ; $\emptyset_s$ =Surface Potential $\emptyset_B$ =Bulk Potential
Parameters extracted from C-V data are tabulated in table1.

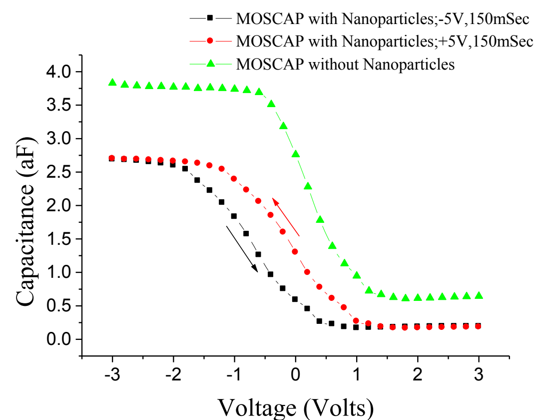


FIG. 2. C-V(1MHz) Curve for MOSCAP Devices

TABLE 1. Parameters for MOSCAP Devices

| | MOSCAP w/o Nanoparticles(NP) | MOSCAP with NP;+5V,150mSec | MOSCAP with NP;-5V,150mSec |
|---|---|---|---|
| **Flat-band Voltage** | 0.84V | 0.73 | 0.1860 |
| **Threshold Voltage** | 1.53V | 1.1V | 0.6V |
| **Oxide Charges** | $3.8\times10^{12}cm^{-3}$ | $4.1\times10^{12}$ $cm^{-3}$ | $3.0\times10^{12}$ $cm^{-3}$ |
| **Cox** | $3.8\times10^{-10}$ | $2.71\times10^{-10}$ | $2.69\times10^{-10}$ |

Characterization of nanoparticles was done with AFM and further image processing with SPIP software (Trial). Details found by the SPIP processing are tabulated in TABLE. 2. FIG. 3. Shows the original AFM image, FIG. 4. is a processed image highlighting the nanoparticles and FIG 5 is a 3D image showing the height of nanoparticles.

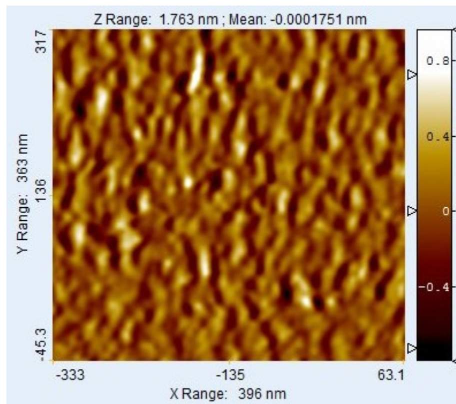


FIG.3. AFM image of Silicon Nanoparticles deposited by LPCVD

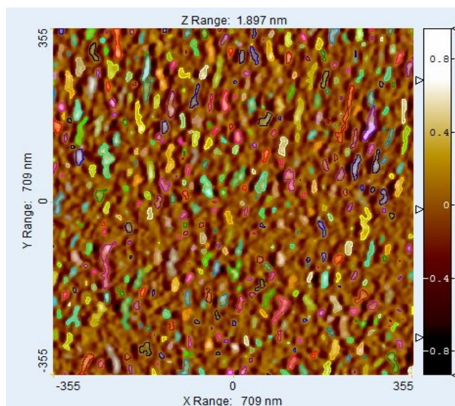


FIG. 4. AFM Image Prcossed by SPIP showing the nanoparticles

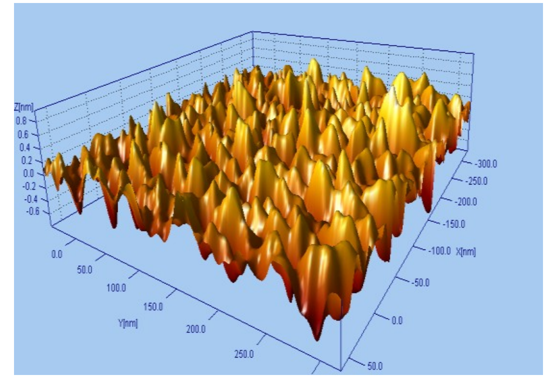

FIG.5. 3D image of Silicon Nanoparticles deposited by LPCVD

TABLE 2 Silicon Nanoparticles' analysis by SPIP

| **Quantity** | **Value** |
|---|---|
| Diameter(min) | 2.005234 nm |
| Diameter(max) | 36.1498 nm |
| Diameter (mean) | 11.22 nm |
| Area (min) | 3.158 $nm^2$ |
| Area (max) | 1026.369 $nm^2$ |
| Area (mean) | 132.258 $nm^2$ |
| Height (min) | 0.209 nm |
| Height (max) | 0.965 nm |

## IV. CONCLUSIONS

The presented paper explores the memory application of silicon nanoparticles. It can be concluded that silicon nanoparticles based memories can be easily fabricated and because of its compatibility with the traditional processing techniques it can be mass manufactured. By controlling the size of nanoparticles charge in MOSCAP can

## V. REFERENCES


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