Recess dependent AlGaN/GaN HEMTs performance

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Abstract

Recess technologies in GaN HEMTs were simulated to check their effect on device performance. Gate recess improved device transconductance. However the drain current reduced. Ohmic recess improved drain current but devices suffered with high gate leakage current. Different recess depths combinations were next simulated. A combination of 10 nm Gate recess together with a 10 nm Ohmic recess showed a balanced good drain current as well as transconductance without any leakage. An optimized critical Gate recess depth in combination to the Ohmic recess depth proved to be a key factor for good I_{ds} and g_m without gate leakage.

Keywords: GaN HEMTs, Gate recess, Ohmic recess, Gate leakage.

Introduction

High transconductance (g_m) and high drain-source current (I_{ds}) without leakage are essential in realizing the full potential of AlGaN/GaN HEMTs for high power, high voltage and biosensing applications. Gate recess is a well-known and a direct method of increasing the device g_m. However, its weak point is the reduction in I_{ds}.

Ohmic recess has proved to reduce the contact resistance and increase the I_{ds} [1]. Therefore the choice of combining the Gate recess with Ohmic recess could bring a simultaneous improvement in both of these parameters. In this paper, we present a detailed simulation work on seperate and combined Ohmic and Gate recess. An analysis on various recess depths is given to achieve an optimized value and combination for good g_m and I_{ds} without any leakage current.

Experimental Result

A non-recessed basic device (A) of 1x100 µm used for simulation had an AlGaN layer of 25 nm and a GaN buffer of 2.7 µm. Table 1 summarizes all types of recess technology cases.

Table 1

Device Technology	**Cases**				
Non Recessed	**A**				
Ohmic Recess (nm)	**B**	**C**	**D**	**E**	**F**
	10	20	25	26.5	1376
Gate Recess (nm)	**G**			**H**	
	10			20	
Ohmic + Gate Recess (nm)	**I**	**J**		**K**	**L**
	10+10	20+10		10+20	20+20

Fig. 1 shows the resulting I_{ds}, g_m and I_g characteristics corresponding to the above Ohmic and Gate recess technology cases. Case H of Gate recess showed maximum g_m (≈ 360 mS/mm) due to highest recorded electric field, mobility and reduced gate channel distance but showed minimum I_{ds}. Case B of Ohmic recess showed maximum I_{ds} (≈ 1.0 A/mm @ V_{gs} =+2.0 V) but together with maximum leakage current I_g. Leakage current in all the Ohmic recess structures was believed to be a component of tunneling current between source and drain due to reduced contact resistance.

Next, in order to obtain leakage free devices having quite good values of I_{ds} and g_m, we analyzed the results of combined Ohmic and Gate recess cases (I, J, K and L). Fig. 1 shows no leakage in these structures. This was probably due to discontinued tunneling component path as a result of Gate recess in combination with Ohmic. Fig. 2 shows the related I_{ds} and g_m graph. In cases of the Gate recess of 20 nm, independent of Ohmic recess depths (Cases K and L), I_{ds} reduced due to a recorded reduction in the Electric Field [2]. However the g_m increased in both of the cases due to reduced gate to channel distance.

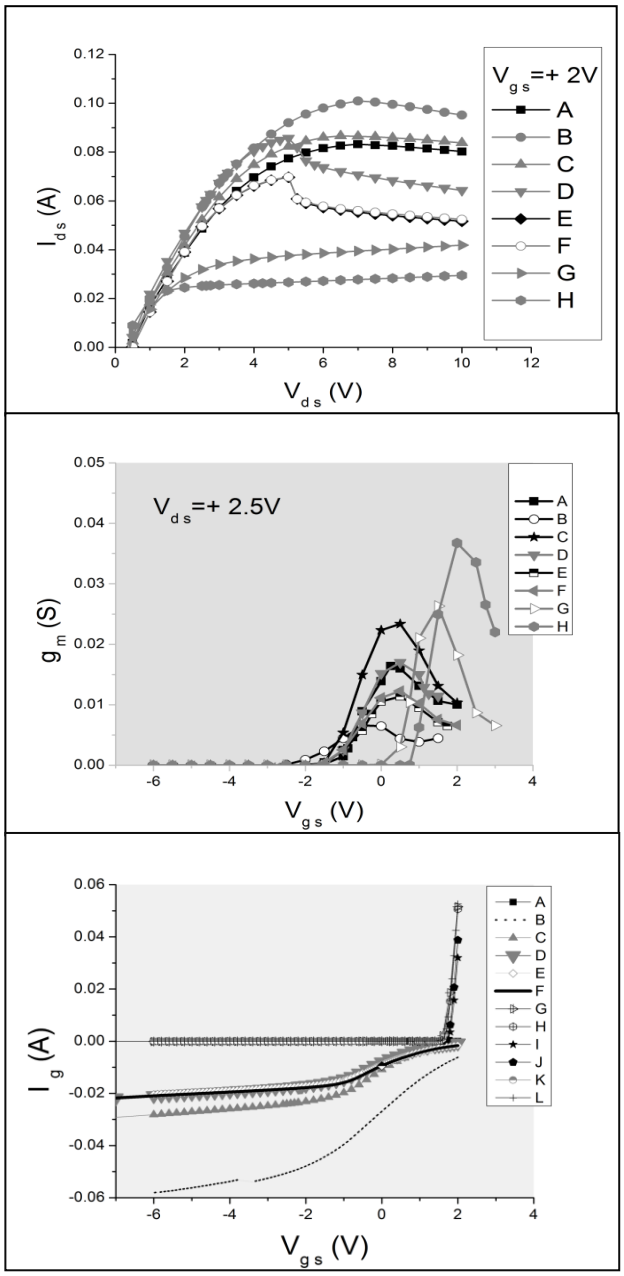

Fig. 1: I_{ds}, g_m and I_g of non-recessed and recessed cases

Interestingly, in cases of gate recess depth of 10 nm, different Ohmic recess depths showed significant differences. A significantly low value of g_m was noted due to reduction in the mobility under gate and gate-drain, when the Ohmic was recessed to a depth of 20 nm with a Gate recess of 10 nm (Case J).

Case I (10 nm, 10 nm) showed a good balance between g_m and I_{ds} without any leakage. Hence, it was considered as an optimum and critical Ohmic and Gate recess depth combination.

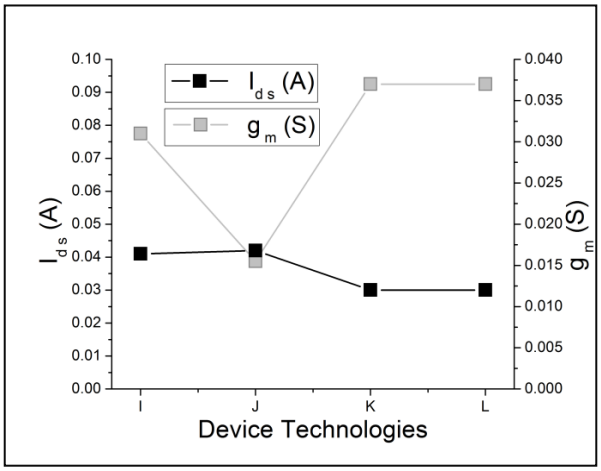

Fig. 2: I_{ds} and g_m of combined Ohmic and Gate recess

Conclusion

Separate and combined Ohmic and Gate recess were simulated to attain good enough values of g_m and I_{ds} without any leakage current I_{gs} Gate recess showed high g_m but reduced I_{ds}. Ohmic recess showed high I_{ds} but with high leakage current. Combined Ohmic and Gate recess technology cases did not show any leakage current. An optimized combined case I (10 nm+10 nm) showed good enough values of g_m and I_{ds} without any leakage. Combined depths could be further optimized to increase the values of g_m and I_{ds} for betterment in the device performance.

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