Silicon Nanowire Arrays using g-line Photolithography

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***Abstract*— 1 and 2 micron wide silicon fin patterns realized using standard g-line UV lithography are oxidized to accomplish nanowires. Simulation results envisage the possibility of silicon nanowire fabrication using top down fabrication approach. Silicon consumption from three sides of the fins reduces their geometries. Stress developed in the oxide leads to a pinch-off in the fins with aspect ratios >3. This pinch-off divides the fin patterns into two parts vertically; upper part converges into silicon Nanowire, buried in silicon oxide. Simulation results for different process temperatures, time and fin aspect ratios are presented in the paper.**

***Index Terms*— Stress Dependent Oxidation, Pinch-off, Fin, Aspect Ratio, Silicon Nanowire**

I. INTRODUCTION

Silicon Nanowires (Si NW) [1] and Carbon Nanotubes (CNT) [2] are being extensively explored for various applications like biological and chemical sensors because of their high surface/volume ratio, Nano-electronics for their fast carrier transport properties and for photonics. Silicon nanowires are also very good temperature sensors because of their high temperature dependency. The presence of charged molecular species on the nanowire surface modulates its conductance. This conductance modulation builds the platform for Bio-chemical sensing [1]. These sensor devices work as Field Effect Transistors (FET) with bio-chemical species as floating gate. Some of the popular ways of making silicon nanowires include chemical vapour deposition techniques to grow SiNW; e-Beam Lithography and deep UV lithography [3, 4] to get silicon fins with nano-dimensional width. Present work demonstrates nano-dimensional Si NWs realized, starting with 1 - 2µm wide Si-fins using traditional g-line photolithography. The concept of stress limited oxidation [5] in the constrained silicon is utilized to reduce micron silicon patterns to nano-dimensions [5, 6].

II. SILICON NANOWIRES PROCESS DESIGN

Silicon fin dimensions and process conditions, to realize nanowires are optimized using Athena Process Simulation Framework of SILVACO. Oxidation method used here is VISCOUS with stress dependency in oxide. Two silicon fins, 1µ and 2µ wide are made on the silicon wafer (p-Type <100>) followed by the stress dependent oxidation. Fins of aspect ratios (AR) 1 to 6 were characterized. For aspect ratio Ó3 it is seen that silicon fins are pinched-off into two parts along its height. This phenomenon is the consequence of reduced oxidation rate due to stresses building, in the upper part of the fin. Stress in silicon oxide [7] affects the parameters in linear-parabolic Deal-Grove model; modified parameters would be expressed as in Eq. 1-3 [7, 8] which suggests that if stress is more the oxidation rate will reduce. This is also called as stress limited oxidation.

$$k_s(stress) = k_s \times exp\left(-\frac{\sigma_n V_R}{k_T}\right) exp\left(-\frac{\sigma_t V_T}{k_T}\right) \quad (1)$$

$$D(stress) = D \times exp\left(-\frac{(P)(V_D)}{k_T}\right) \quad (2)$$

$$C^*(stress) = C^* \times exp\left(-\frac{(P)(V_s)}{k_T}\right) \quad (3)$$

Where k_s is normal interface reaction rate, $\mathring{u}_n$ is stress normal to the growing interface, $\mathring{u}_t$ is the stress tangential to growing interface, D is the normal oxidant diffusivity, C^* is normal oxidant solubility and P is the hydrostatic pressure in the growing oxide; V_R, V_T, V_D and V_s are considered to be stress dependent activation volumes.

The upper part of the fin is totally isolated from the wafer later on by removing the oxide; these hanging nanowires can be used for sensing applications. Size of this oxide buried wire can be controlled with oxidation time and temperature. Silicon consumption during thermal oxidation reduces the dimension of the wire and nano dimensions are reached. Simulation suggests the nanowire formation in 1µm wide fin with AR 3, as thermal oxidation progresses [Fig. 1]. Higher AR leads to early pinch off and reduced geometry of nanowire for the same oxidation time. Figure 2 shows nanowire cross-sections 109nm × 656nm and 53nm × 360nm with starting 1µm wide fins having AR 3/1 and 6/1 respectively after 5 hours of wet oxidation at 1000°C.

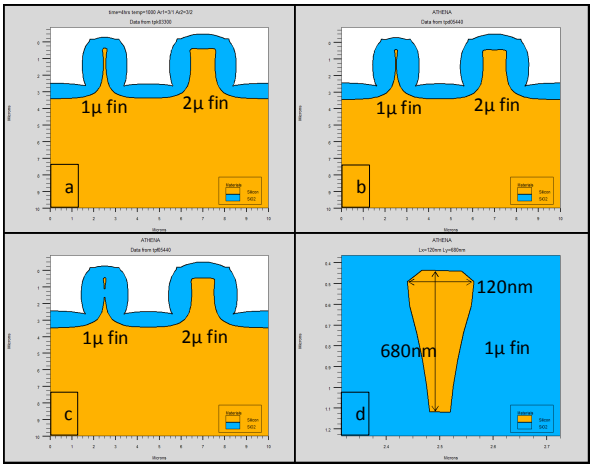

FIG. 1. Simulation results of 1µm and 2µm wide fins with AR 3/1 and 3/2 respectively, after wet oxidation at 1000ºC for (a) 4hour, (b) 4hour 40min and (c) 4hour 50min; (d) isolated nanowire (120nm x 680nm) formed after 4hour 50min of wet oxidation in 1µm wide fin due to pinch-off process.

The fin critical dimension (CD) where pinch-off initiates is investigated as a function of fin AR. 10hours of wet oxidation at

1000ºC in 2µm wide fins leads to CD of 625nm and 350nm in fins having AR 1.5 and 3 respectively [Figure 3].

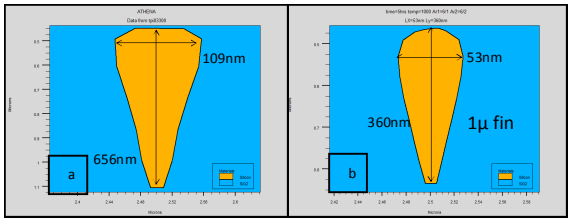

FIG. 2. Isolated nanowire with cross-section (a) 109nm × 656nm and (b) 53nm × 360nm formed with 1µm wide fins having AR 3/1 and 6/1 respectively after 5hours of oxidation at 1000ºC.

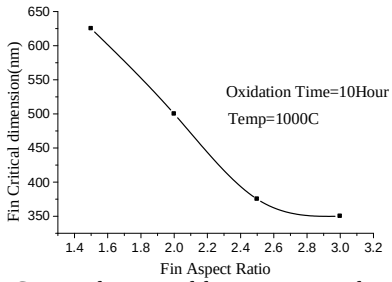

FIG. 3. Fin CD as a function of fin aspect ratio after 10hours of oxidation at 1000ºC.

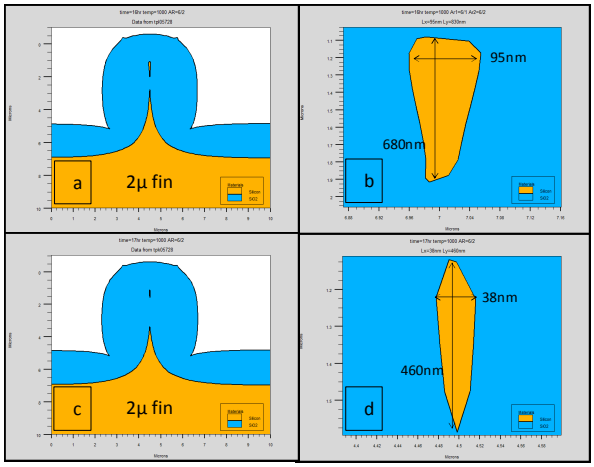

FIG. 4. Nanowire in 2µm wide fins after wet oxidation at 1000ºC for (a) 16 hours, (b) Zoomed NW after 16 hours (95nm × 830nm), (c) 17 hours, (d) Zoomed NW after 17 hours (38nm × 460nm).

2µm wide fin also pinch-off to give Si NW after ~16 hours of wet oxidation which can be further reduced in dimensions by oxidation. As is well known, the oxidation rate deteriorates with the SiO_2 growth on the Si surface. Silicon consumption from the finôs vertical walls (both sides) as a function of time is in figure 5. This plot suggests silicon consumption rate linear, up to 4hours of oxidation while there after reduced slope limits the silicon consumption rate. The long process time can be reduced by stripping SiO_2 intermittently during oxidation as indicated in Table-1. 2µm wide fin with AR 3 is subjected to wet oxidation for different time intervals with SiO_2 stripped in BHF after each oxidation step. Total time is estimated till the pinch-off initiates.

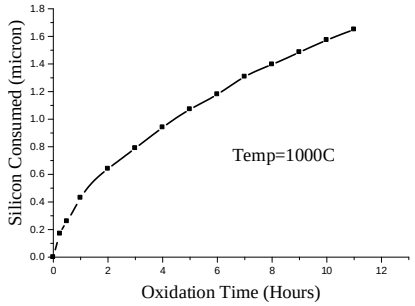

FIG. 5. Silicon consumption increases fast up to 3 to 4 hours after that rate goes down.

TABLE 1. Pinch-off time with multiple oxidation steps; SiO_2 stripped in HF after each oxidation step.

Oxidation Steps	Total Time for Pinch-off (Hours)
Single	16
Double	5 + 4 or 4 + 5
Three steps	3 + 3 + 1.17

III. NANOWIRE FABRICATION

Nanowires in array format [Fig. 6] are being fabricated using CMOS compatible processes which include defining fin patterns using g-line photo-lithography, followed by Deep Reactive Ion Etching (DRIE), wet oxidation to get Si Nanowires as mentioned in the process design, etc. The complete fabrication process including metallic inter-connects and passivation layers and various structural and electrical characterizations will be presented.

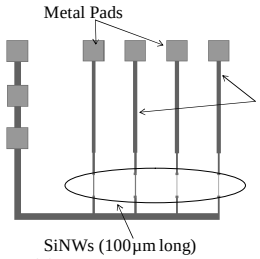

FIG. 6. Schematic layout of four Silicon Nanowires.

IV. CONCLUSIONS

Silicon nanowires fabrication process using the tradition top down approach is optimized using Athena simulation. The reliable technology is being used to realize SiNW arrays suitable for various sensor applications. Silicon nanowires fabricated by CMOS technology have the advantage of integration with standard signal conditioning circuits.

V. REFERENCES

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