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AFM BASED NANO-PATTERNING PROCESS INTEGRABLE WITH MICRON SIZE FEATURES

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For developing nano-scale devices, nano-patterns and their processes should be compatible and integrable with the rest of the fabrication processes. Nano-patterning experiments have been carried out using 16-Mercapto Hexadecanoic Acid molecular ink on fabricated smooth gold film surface using Dip-Pen-Nanolithography technique. Process methodologies have been designed to integrate nano-patterns with micron-size interconnection lines and contact pads. Thin Ti (~10nm)/Au(~50 nm) metal films with low roughness (~1nm) have been deposited on SiO_2/Si substrates by e-beam evaporation. Micron size pads have been patterned with photolithography followed by metal etching. A small window (6 μm X 6 μm) was opened at the centre of pattern by another photolithography step. Nano-writing process was carried out, through self-assembly of compatible 16-MHA ink on gold surface. Experiments have been carried out with different speeds under varying humidity and temperature conditions. Minimum line width of ~53 nm was estimated from lateral force microscopy image. The experimental results indicate strong potential of AFM -based process in the fabrication of nano-structures such as nano-gap electrodes, which is the basic platform for nanoelectronic/ molecular devices.

Keywords: Atomic force microscopy, Dip-Pen-Nanolithography, nano-patterning, nano-gap electrodes, nano-electronic/ molecular devices.

1. Introduction:

Scanning probe microscopy, in addition to imaging, is becoming important tool for new challenges in patterning for nano-scale devices/circuits [1]. There are various nano-patterning techniques namely, electron-beam (EBL), extreme UV, X-Ray, nano imprint lithography and focused ion beam lithography [2]. Scanning tunneling microscopy has been used to manipulate atoms. Atomic force microscope (AFM) has been used to scratch nano-lines on soft materials films [3]. Recently, AFM based technique has been introduced to write pattern/deposit different materials on compatible substrates for different applications [4]. This technique, known as dip-pen-nanolithography (DPN), relies on molecules diffusion through water meniscus. The meniscus is formed between AFM tip and substrate under environment humidity, as tip scans the substrate surface. The desired molecules are deposited as self-assembled monolayer (SAM) due to chemisorption on the surface. The DPN technique has been used to pattern various materials on compatible substrates [5]. Bias voltage may be applied between tip and substrate to oxidize locally the surface-layer of the substrate and thus, creating tunnel barrier for quantum effect based nano-devices such as resonant tunneling diode and single electron transistor.

There is a need to develop nano-patterning process, which is compatible with other processes in device fabrication. The new generation of nano-/molecular devices requires fabrication of nm spaced source and drain, and nano- dot/wire is deposited or positioned between them for electrical measurements [6]. We have carried out nano-patterning (lines, triangular

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electrodes etc.) experiments using 16-Mercapto Hexadecanoic Acid (MHA) molecular ink on gold thin films. Integrated process and mask layout have been designed for such device fabrication and initial experiments have been carried out. Few results are presented and discussed in this paper.

2. Experimental Procedure:

N-type, <100>, low resistivity silicon wafers have been used in fabrication process. Thin thermal oxide was grown using dry oxidation. Ultra-thin Ti (10nm) / Au(50nm) films were deposited by electron beam evaporation using controlled process parameters in order to get low surface roughness [7]. Nanowriting of 16-MHA molecular ink was conducted on these substrates using DPN NSCRIPTOR system procured from NanoInk, USA. Horizontal and vertical lines and triangular electrodes were patterned. Real nano-scale device fabrication requires multiple of lithography and etching steps. This needs registration and alignment at each lithography level. The substrate contains several device patterns, and nano-writing is performed at one of these locations at a time (serial process possible with single AFM tip system). This necessitates the address-ability of each device on the wafer. To tackle this problem, addressable mask levels and fabrication process have been designed for integration of micron size pads/lines with nano-pattern. To check the feasibility of the design, fabrication process was carried out to generate nano-lines connected with micron size pads/connect lines.

3. Results And Discussions:

AFM image of surface of fabricated Ti/Au film on silicon substrate is shown in figure 1 below. The measured surface roughness is ~1.0 nm.

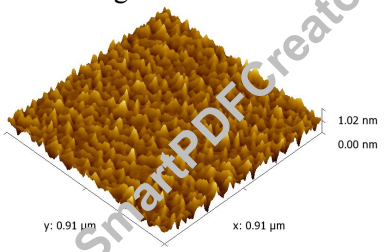
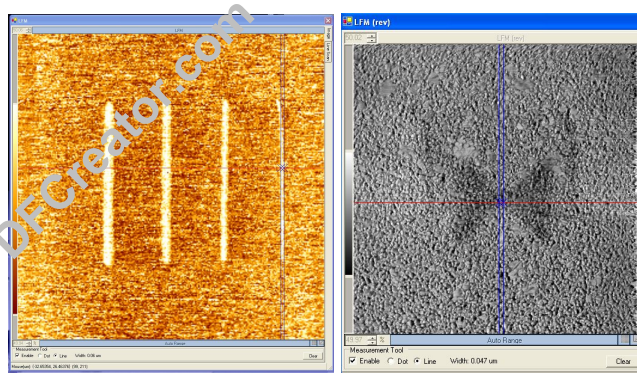


Fig. 1: AFM image 3-D view of surface of Ti/Au film deposited by e-beam evaporation.

Line patterns were written using 16-MHA on commercial and fabricated substrates. Nano-writing process involved AFM tip coating with ink, ink testing and calibration, under different humidity and temperature conditions.

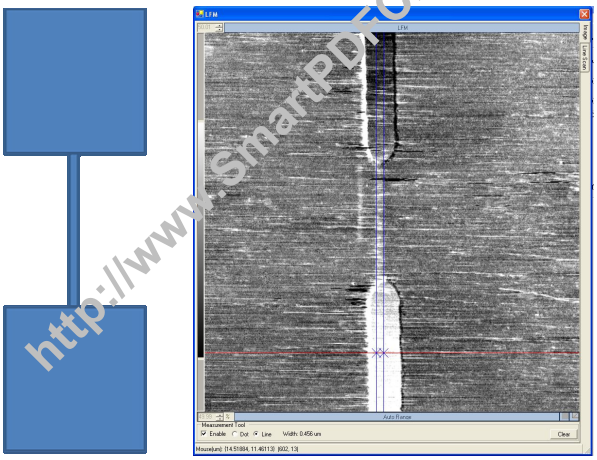
The calibration parameters are used in nano-writing process. Lines were written at different speeds 0.1 - 1.2 µm/sec. Figure 2 (a) shows LFM images of line written at Temp.=24^{0}C, R.H.= 36%. For speed of 1.2 µm/sec, the line width is 60 nm. Triangular nano-gap electrodes patterns were also written in 1 µm area using these parameters. LFM image is shown in Fig 2(b), estimated gap is ~50 nm.



(a) (b)

Fig. 2: Vertical lines written on gold substrate, using calibration parameters (a) and triangular electrode pattern written in 1µm x1µm area (b).

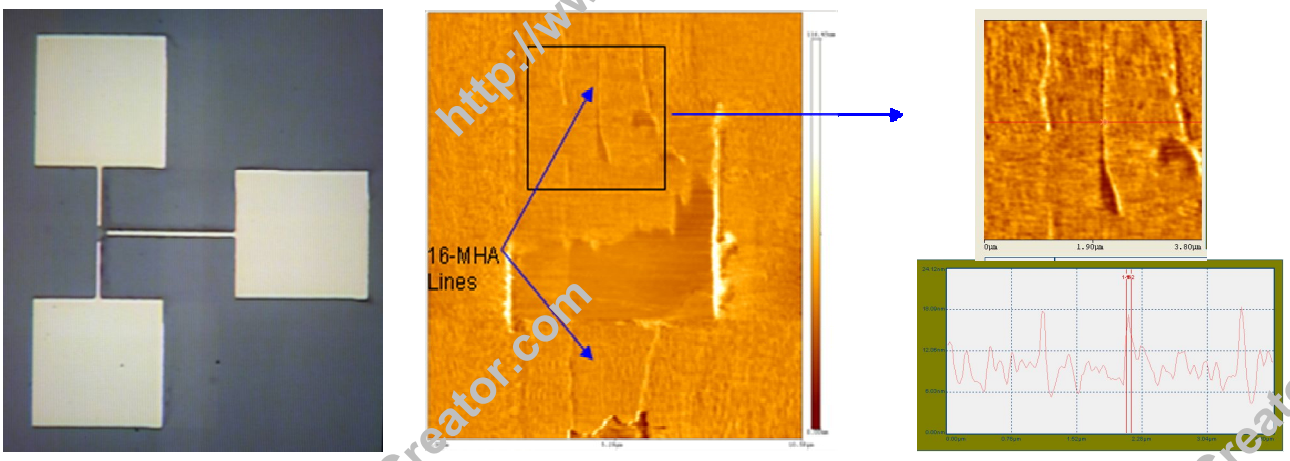
After these experiments, integrated fabrication process for planar nano-gap electrodes structure was undertaken. Experiments were designed to check feasibility of integrating micro- and nano- lithography process using single metallization step. Designed micro pads/lines structure is shown in figure 3(a). LFM image of line written between these connect lines is shown in fig 3(b), written line is clear and continuous. The measured width of drawn line is 456 nm under these process conditions. This process demonstrates the integration of nano- and micro features in MOS environment.



(a) (b)

Fig. 3: Designed micron size pads and connecting line (width =3 µm) (a) and LFM image of line of 16-MHA written between addressable electrodes (b).

Further experiments were conducted on specially fabricated Au/Ti/SiO_2/Si substrate with comparatively thick Au film, needed on pads/connect lines. Simultaneously, ultra-thin Au film is required in DPN window for writing and etching of nano patterns. Contact pads/connect lines were defined through photolithography and metal etching. A 6µm x 6µm window was opened at the center of this micro pattern through another photolithography step. Gold was partially etched from this window. This step resulted in very thin (~15nm) gold layer in DPN window and at the same slightly thicker layer on pads and connect lines, required for contact purpose. Several writing experiments were conducted in this window under different process conditions. Optical micrograph of electrode structure with partially etched gold film is shown in fig. 4(a). LFM image of one such nanowriting experiment carried out at 25^0C and 65% R.H. using 16-MHA is shown in figure 4(b). It was observed that line was visible, though very dim. Estimated line-width (in NanoRule module) is 53 nm. But it was also observed that the line is not continuous rather broken as shown in fig. 4(c). We understand that gold surface is damaged during chemical etching. The nanowriting process is very sensitive to surface condition and process parameters. For good nanowriting process surface should be clean and free from any adsorbents.



(a) (b) (c)

Fig. 4: Optical image of micron size electrodes, pads and DPN window after first level photolithography and partial gold etching (a), LFM image of 16-MHA line written between addressable electrodes on partially etched gold film in DPN window (b), and enlarged view of the written line and profile for width estimation (c). Designed line width – 50 nm, measured line width ~ 53 nm.

4. Conclusions:

AFM based nano-patterning using 16-MHA on fabricated Au/Ti/SiO_2/Si substrates, has been carried out with line-width of 60 nm. Process and addressable mask layout has been designed for integrating nano-pattern/process with micron size pads/connect lines in standard MOS process. Fabrication steps have been carried out. Lines of 53 nm and 456 nm width have been written using 16-MHA in addressable DPN window. These lines are connected with pads through 3 μm lines. Further efforts are underway to develop process for clean and smooth surface in DPN window for controlled writing and etching. These experimental results will be useful for development of nano-/molecular devices.

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