Design of Pseudo Flip-around Sample- Hold Circuit for 10-bit, 5-Msamples/Sec Pipeline ADC

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Abstract: This paper describes the design of a pseudo flip-around sample- hold circuit for a 10-bit, 5-Msamples/sec pipeline ADC. The sample-hold circuit is simulated in 0.35 µm Austria Microsystems technology with a 1 KHz, 1.2 Vp-p sinusoidal input and a sampling clock of 5 MHz. The simulation shows a worst case sampling error of 1 mV, SNR of 60 dB. The layout of the sample hold circuit occupies an area of 0.007mm^2 and consumes 1.7 mW of power.

Keywords: Sample-and-Hold, ADC, SNR, Flip-around

I. INTRODUCTION

Modern applications such as LAN transceivers, broad band communication systems require high speed, high throughput and higher resolution analog-digital converters (ADC) [1]. Constant scaling of transistor has further increased the band-width of operation demanding higher resolution ADC with improved throughput. In literature various architectures of ADC has been proposed [2, 3]. Pipeline ADC is most suitable for high speed application [2]. In conventional cascaded pipeline ADC [4] each block consists of a sample-hold circuit along with other components like amplifier and comparator. Transient simulation of typical sample-hold circuit used in each block is shown in Fig.1. As sample-hold circuit is in hold mode, DC gain limitation of op-amp will create an offset at the output. Phase Margin (PM) and Gain Band-Width (GBW) of op-amp limit the overall frequency response of sample-hold circuit. The settling time of a sample-hold circuit with feedback capacitor can be mathematically expressed as following [2]:

$$V_o(t) = V_o(t_o) - \frac{\alpha V_i}{1 + \frac{1}{\beta A_v}}\left[1 - e^{-WGBWt}\right] \quad (1)$$

$V_0(t)$ is the output voltage of the system in time domain.

Where $W_{GBW} = \frac{\beta g_m}{C_{tot}}$

α=1 (for well matched capacitor)

β= *feed-back factor*

$A_v = g_m / g_0$ *(open loop dc gain)*

"β" plays a major role in determining settling time of circuit. Settling time of sample-hold circuit can be decreased by increasing GBW or decreasing DC gain A_V which can be seen from equation(1). In both the cases high performance op-amp is required. High performance op-amp demands complicated compensation techniques due to multiple stages and also results in larger area. However, by enhancing feed-back factor (β) dependency of a sample-hold circuit on op-amp parameters can be reduced.

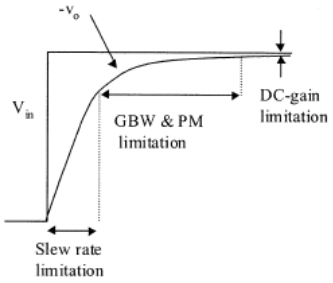

Fig.1: Transient Output of S/H Circuit

Transient simulation shown in Fig.1 is having a gain error or output offset. Various architectures [5] have been proposed to reduce the output offset voltage associated with sample-hold circuit. All these architectures use complex switches to compensate the error produced due to switching activity and gain error. These complex switches increase design complexity and require additional clock routing. Hence in the proposed work, output offset of sample-hold circuit is controlled by an offset compensating switch. Offset compensation is achieved by sampling offset in sample mode & subtracting it from the signal in hold mode.

Various architectures [6] have been proposed to enhance "β". Flip-around sample-hold architecture is widely used due to "β" enhancement from the architecture. Flip-around architecture use high performance switch for switching the capacitor, which demands low charge injection switch with minimum on

resistance [7]. Output offset of Flip-around sample-hold circuit is controlled by Common Mode Feedback (CMFB) circuit. In the proposed circuit one of the capacitor is flipped with clock phase to enhance feedback factor and minimize output offset, whereas the input capacitor position remains fixed. As offset minimizing switch in conjunction with movable feedback capacitor uses both the benefits of traditional and flip-around sample-hold circuit, the proposed architecture is named pseudo flip-around S/H circuit. The typical output offset of the proposed sample-hold circuit is less than the minimum required resolution for a 10 bit pipeline ADC. Hence, the proposed S/H circuit can be used in a 10 bit pipeline ADC.

Section II describes the working of proposed topology. "β" enhancement with its application and Offset control by a switch are described in section III. Finally, the total design of the proposed sample hold circuit is simulated in AMS 0.35 µm technology (2-poly, 3-metal) and simulation results are presented in section IV.

II. WORKING OF PROPOSED TOPOLOGY

Pseudo flip-around sample-hold circuit consists of two capacitors *C1* and *C2* each valued 0.5pF, a two stage miller compensated op-amp, two de-multiplexers and a switch as shown in Fig.2. The circuit works in two non-overlapping clock phases' $\phi 1$ and $\phi 2$.

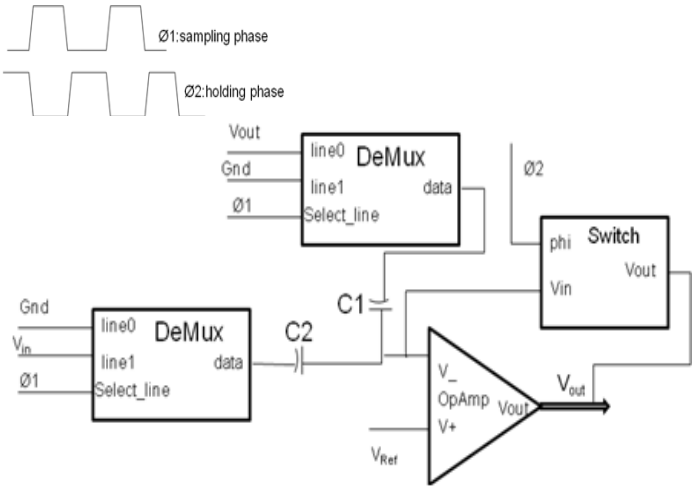

Fig.2: Pseudo Flip-around S/H Circuit

The non-overlapping clocks are as shown in Fig.2. In phase $\phi 1$, the circuit is in sampling mode as shown in Fig.3 (a). In sampling mode, left plates of capacitors *C1* and *C2* are switched to 'Ground' (zero potential) and input voltage (V_{in}) respectively in contrast with previous implementation of the same architecture [8]. So, during this phase the left plates of *C1* and *C2* are charged to Ground and V_{in} with the help of virtual node created by amplifier A in buffer mode as shown in Fig.3 (a). In the hold phase $\phi 2$, the left plate of *C2* is connected to Ground and the capacitor *C1* is switched around the amplifier as shown in Fig.3 (b). With reversal of polarity of capacitor, the charge across *C1* is subtracted from total charge at the output node. Thus output voltage is sampled to input voltage. The above switching of capacitors *C1* and *C2* are done with the help of two demultiplexers (DeMux) as shown in Fig.2. Switch is used to store the offset of op-amp in the sampling phase i.e. when the amplifier is in buffer mode as shown in Fig.2. The "β" enhancement and offset cancellation with the use of switch is described in detail in the next section.

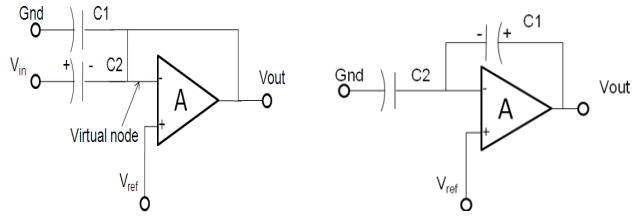

Fig.3 (a): S/H in Sampling Mode (b): S/H in Hold Mode

III. "β" ENHANCEMENT WITH ITS APPLICATION AND OFFSET CONTROL BY A SWITCH

Equation (1) gives a relation between "β" and $V_O(t)$. $V_O(t)$ can be minimized by increasing "β". Feed-back factor "β" plays a crucial role in determining overall variation of virtual node at inverting terminal of op-amp. Stability of virtual node determines the accuracy of charge transfer from *C2* to *C1* in Fig.3(b). The effect of feedback factor on the S/H circuit can further be analyzed by its ac small signal equivalent which is shown in Fig.4. For simplicity we have neglected the capacitive elements from the equivalent circuit. As shown in Fig.4, the feedback element of the S/H circuit is approximated by a two port equivalent network. Similarly, the amplifier is also represented by its macromodel. We know that gain of a feedback circuit is dependent on feedback element [9]. In the proposed S/H circuit, the feedback element consists of a switch which leads to an additional impedance factor. Moreover, the switch impedance is having a frequency dependency. So, the effect of feedback factor on the overall gain of the S/H circuit can be theoretically derived from Fig.4 and can be expressed as:

$$A_f = A_i / \{1 - T\} \qquad (2)$$

Where,

$$T \approx -A_i \left[r_i R_f / \{ R_i + (r_i \,||\, R_f) \} \right] R_L / R_f$$

T is the loop gain, A_i is the open loop gain of op-amp without feedback, A_f is gain with feedback, r_i is impedance of source, R_i is impedance of amplifier, R_f is impedance of feedback element with switch and R_L is load impedance. R_f is a frequency dependent component and changes with input frequency. Frequency dependency of R_f comes from the switch capacitances. The channel resistance "*R*" of switch is minimized by a parallel connection of transistor as shown in Fig.5.Reduced channel resistance of implemented switch helps in equalizing $f_{3\text{-}db}$ with f_{GBW} in buffer mode ("β" = 1). Feedback factor enhancement reduces bandwidth requirement of op-amp. An op-

amp of sample-hold circuit used in an ADC [10] must have bandwidth equal to:

$$f_{3-dB} > \{2^{(N-1)/2}\} f \quad (3)$$

Where "*N*" is the number of bits and f is the input frequency. $f_{3\text{-}db}$ must be enhanced for higher resolution ADC. An op-amp in feedback will have a different scenario. Here the switch plays a major role (switched circuit).

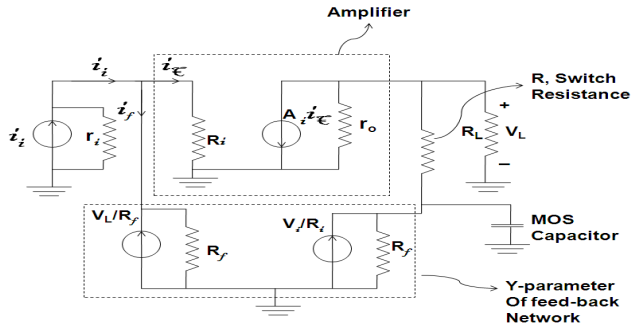

Fig.4: AC Small Signal Equivalent of S/H

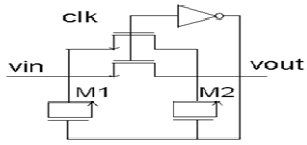

Fig.5: Switch Architecture

Consider the following equation:

$$f_{3-dB} = \frac{1}{2\pi R_{on}\left(C_{ss} + C_{ps} + C_{ps}\right)} \quad (4)$$

Where C_{ss}, C_{ps} and C_{pd} are the junction capacitances associated with gate, source and drain of the switch transistor. By reducing R_{on}, $f_{3\text{-}db}$ can be increased. Consider the equivalent model of switch as shown in Fig.6. Here R_{chn} is the channel resistance of switch. The R_{on} can be represented in terms of two NMOS switches.

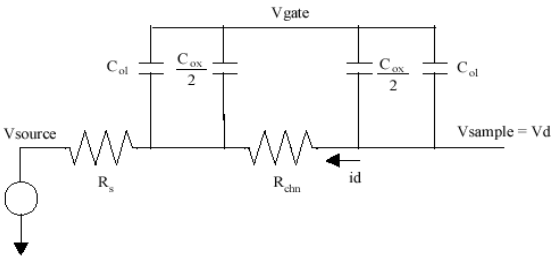

Fig.6: AC Small Signal Equivalent of Implemented Switch

$$R_{on} = 1/\left\{\begin{array}{l}\mu_{n1}C_{ox}[W/L]_{n1}(V_{DD} - V_{tn1}) - \\ (\mu_{n1}C_{ox}[W/L]_{n1} - \mu_{n2}C_{ox}[W/L]_{n2})V_{in} - \\ \mu_{n2}C_{ox}[W/L]_{n2}\,|V_{tn2}|\end{array}\right\} \quad (5)$$

The total bandwidth is controlled by adjusting R_{on}. The amplifier whose macromodel is shown in Fig.4 is implemented by a traditional two stage op-amp as shown in Fig.6.

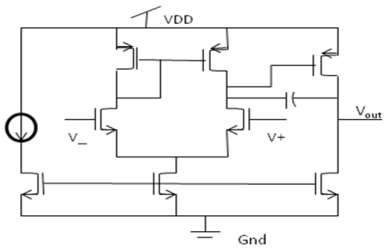

Fig.6: Architecture of Operational Amplifier (op-amp)

Offset of sample-hold circuit is reduced by the dummy capacitors (M1, M2) which are implemented by MOSFET as shown in Fig.5. The dummy capacitors are used to store offset voltage associated with output node in the sampling phase of S/H and which is subsequently negated in the hold phase as described in SectionII. Another source of offset alteration is the error introduced by clock feed-trough phenomena of switch. The channel charge is neutralized by the dummy switch but the spike produced by C_{ox} due to clock is not best controlled by the dummy switch. So, during transient analysis a spike is observed during clock phase change.

IV. SIMULATION AND RESULTS

The transient simulation result of the sample-hold is shown in Fig.7. The DFT result is obtained by applying a 1 KHz sinusoidal input with 5MHz sampling frequency. The result is shown in Fig.8. Monte-Carlo simulation of sample-hold circuit is shown in Fig.9. In Fig.9, output of a random input is shown. In the x-axis random voltages of input are shown and they are numbered (1-16).

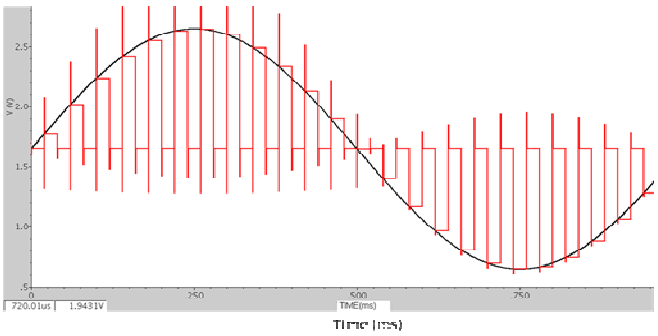

Fig.7: Transient analysis of S/H circuit showing output and input signals

The corresponding output voltage is shown in Y-axis. The maximum and minimum deviation of sampled voltage from the input voltage is shown by output voltage (1) and output voltage (2). Process variation result showed a maximum variation of 2 mV in output voltage. The total area occupied is around 0.007 mm^2. Total power consumption is 1.7mW. Proposed circuit is operating at 5 MHz sampling frequency and this is typical

operating frequency of CMOS image sensor application. Comparison of proposed design with previous work is done in table1.

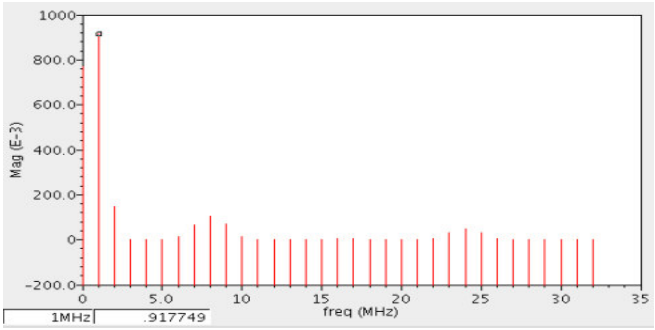

Fig.8: DFT analysis of S/H circuit output

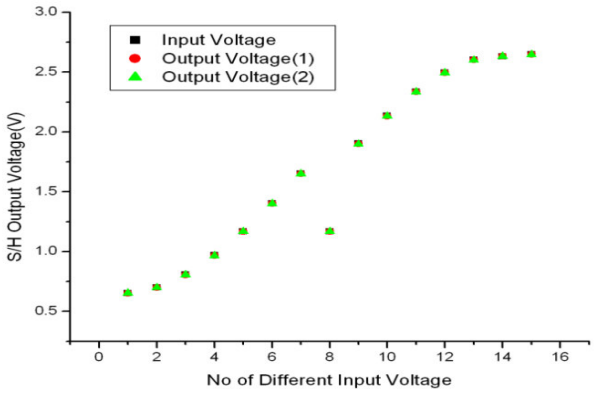

Fig.9: Monte-Carlo analysis results

V. CONCLUSION

A novel compact sample-hold circuit is proposed. The total area occupied is 0.007 mm^2. In the current work switch is used to reduce design complexity. Monte-Carlo simulation of sample-hold shows a maximum output voltage variation of 2 mV. The simulation results show that proposed sample-hold can be used in a 10-bit pipeline ADC operating at 5 MHz. Proposed circuit can be implemented for medical image application.

TABLE -1

Parameters	**Value [proposed]**	**Value [7]**
Sampling Rate	5 MS/s	50 Ms/s
Resolution	10 bit	10 bit
SNR	60 dB	62 dB
Input Range	1.2 V	1.6 V
Supply Voltage	3.3 V	3.3 V
Power Consumption	1.7 mW	13.6 mW
Active Area	0.007 mm2	0.12mm2
Process	0.35 µm	0.35 µm

VI. REFERENCE

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