ISFET FABRICATION AND DESIGN OF ON-CHIP READOUT CIRCUIT USING 0.35μm DIGITAL CMOS TECHNOLOGY

*M.D.Prakash, *M.Santosh, *V.K.Khanna

*Central Electronics Engineering Research Institute (CEERI)/Council of Scientific & Industrial research (CSIR), Pilani-333031 (Rajasthan), India

Abstract: - Biomedical instruments are widely used in modern medical facilities. Among these instruments, pH measurement is a vital biomedical application. Biomedical sensors like ISFET are used to detect the pH level. In the current work, a detailed explanation of the ISFET fabrication is discussed. The fabricated ISFET by the proposed method is characterized. After characterization, I_D curve is plotted for different pH solutions. A macro-model of the fabricated ISFET is prepared. This macro-model is used to design a readout and bias circuit. The bias circuit is used to provide constant current to ISFET, the current is controlled by a resistor. An op-amp is used to source current. The output is taken through a differential amplifier. The output is almost rail to rail (3 V for 3.3 V supply). The op-amp used has a PSRR of 65 db and resistor used to control current is made process independent by parallel-series splitting of a poly-silicon resistor. The total circuit is simulated in cadence software using AMS (Austria Micro System) 0.35 μm technology having 3 metal layers and two poly-silicon layers.

I. Introduction

Ever since its invention, biosensor like ISFET (Ion Sensitive Field Effect Transistor) has been used for pH measurements. In literature [1], it is seen that ISFET is fabricated separately and read-out circuit is connected externally to extract the output voltage. With the advent of compact biomedical instrumentation, biomedical circuit integration with traditional CMOS circuit is a major challenge for modern SOC designer. The accelerated rate of technology scaling has created additional challenges in fabrication of biosensor with conditioning circuit. Traditionally biosensors are off-chip modules [2] but demand of low power systems has forced integration of sensor with conditioning circuit. In the current work, ISFET based biosensor is used to detect pH level. The ISFET can be considered as a special type of the MOSFET without a metal gate, by which, the gate insulator is directly exposed to the analyte solution. A change of the surface potential between electrolyte and insulator will result from a change of pH concentration in the electrolyte. In view of its very small size, rapid response and compatibility with

standard CMOS process and low cost, it offers several advantages in comparison with a conventional ion-sensitive electrode particularly in the compact and highly sensitive biomedical applications [3].

In the current work, fabrication of ISFET and design of on-chip read-out circuit is presented using 0.35 μm digital CMOS technology. Complete work is divided into four sections. ISFET design and fabrication are explained in Section-II. Characterization and macro-modeling are done in Section-III. Readout circuit is explained in Section-IV. Results are explained in Section-V and conclusions are discussed in Section-VI.

II. ISFET design and fabrication

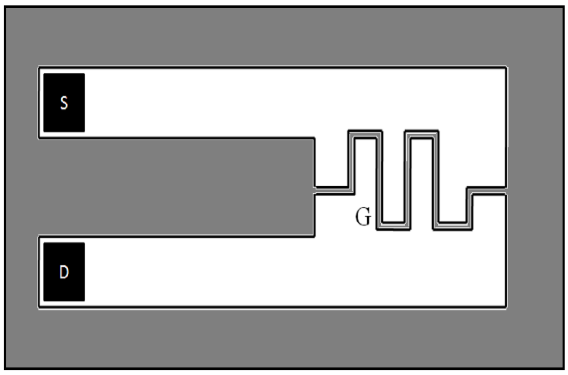
The principle of measuring the concentration of chemical quantities with a solid-state device, called ISFET, was introduced in 1970 by P. Bergveld [1]. ISFET fabrication is partially based on the standard CMOS fabrication process. The main design parameter is the aspect ratio i.e ratio of channel width "W" with channel length "L" of ISFET. This ratio controls the current through the sensor. Trans-conductance of an ISFET is defined as-

$$g_m = \frac{\delta IDs}{\delta VGS} \Big| V_{DS}=\text{constant} \qquad (1)$$

For higher "g_m", more is the drain-source current change produced by a given gate-source voltage change at a fixed drain-source voltage, and therefore more effective will be the interfacial potential acting on the gate of the ISFET. In the present device, the channel length as 12 μm and channel width as 4800 μm giving an aspect ratio of 400 [4]. The effect of W/L ratio on the MOSFET transconductance "g_{ms}" in the saturated condition is represented by the equation

$$g_{ms} = \mu_n \left(\frac{W}{L}\right) C_d (V_{GS}-V_{TH}) \qquad (2)$$

where μ_n is the electron mobility on the surface (700 cm^2/Vs), C_d is the capacitance per unit area of the gate dielectric ($=2.12\times10^{-8}$ F cm^{-2}, for the present device), V_{GS} is the gate-source voltage and V_{Th} is the threshold voltage of the device. For V_{GS} - V_{Th} = 1V, g_{ms} =5.6 mA/V = 5.6 mS. The geometrical layout of the transistor on the ISFET chip is illustrated in figure-1.



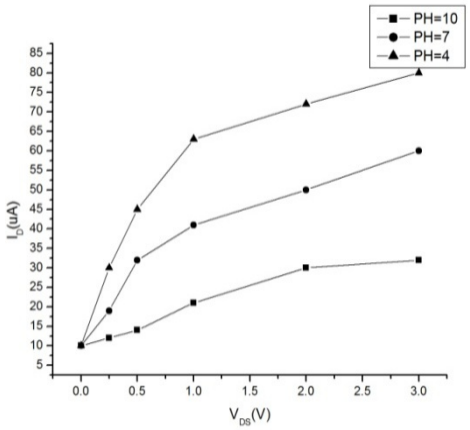
(Fig. 1. ISFET layout)

Fabrication technology of proposed ISFET is based on the traditional CMOS fabrication technology [4]. The ISFET has been fabricated using metal-gate NMOS transistor on a P-type silicon wafer. The resistivity and orientation of p-type wafer is 15–20 Ω-cm and <100>. ISFET fabrication consists of a four-mask level process. The first photo masking step opened the source and drain diffusion windows. In the second photo masking step, the gate window has been opened followed by gate oxidation and silicon nitride deposition. Trichloroethylene oxidation has been used. The third and fourth photolithography steps were for the contact window opening and metal pattern delineation respectively. After epoxy

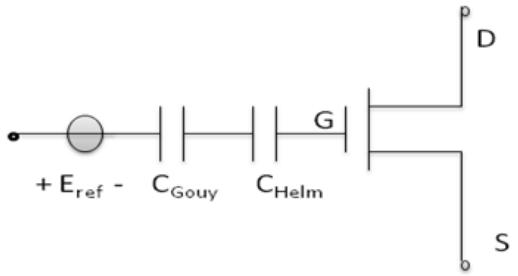
protection, only the gate area was left exposed.

III. Characterization and Macro-modeling-

Fabricated ISFET is characterized using an *I-V* tester. The drain voltage variations with different gate voltage (pH solutions) are plotted in figure-2. The macro-model is designed by assuming that the total ISFET can be partitioned as two fully uncoupled stages, electronic stage(starting structure MOSFET) and electrochemical stage (electrolyte-insulator interface). Under the assumption of charge neutrality, electrochemical stage can be considered as uncoupled from the electronic stage. By applying site-binding theory and electrical double layer theory [5], ISFET equivalent/macro-modeled circuit can be represented as shown in figure-3. Macro-model can be used for co-simulation with read-out bias circuit. The current macro-model is not having any noise information of ISFET sensor.



(Fig. 2. I_D V_s pH value)



(Fig. 3. Macro-model of ISFET)

IV. Read-out Circuit-

In the proposed read-out and bias circuit, a constant current source is implemented using op-amp and an on-chip process insensitive resistor [6]. The performance parameters of the op-amp used are listed in Table-1. The drain current through the ISFET is controlled by the resistor. Mathematically, current can be represented as following-

$$I = V_{REF}/R \qquad (3)$$

Resistor "*R*" is implemented by series-parallel combination of poly-silicon resistors. Resistor can be made temperature independent to some extent by modifying number of resistors in series-parallel arrangement [7]. Consider the following mathematical representation of thermal co-efficient "*TC*"-

$$TC_{SP} = TC_B + \frac{(T_{CA} - T_{CB})(\alpha_{sp}\,\beta_{sp})}{(1+\beta_{sp})(1+\alpha_{sp}+\beta_{sp})} \qquad (4)$$

Where:-

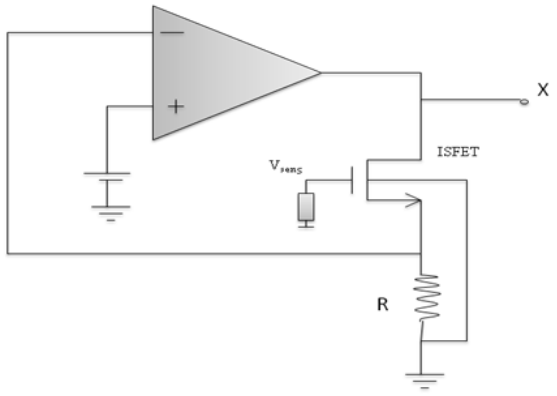
sp = series/parallel

$\beta_{sp} = R_A/R_B$

$\alpha_{sp} = \beta^2 - 1$

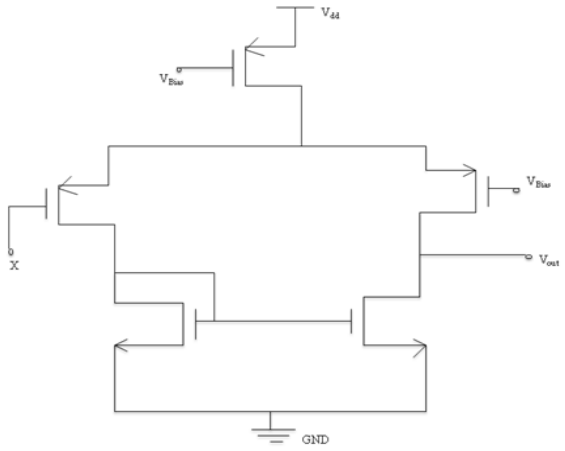
From the above equation, "*TC*" of resistor "*R*" can be stabilized by optimizing "R_A" and "R_B". Complete bias circuit (op-amp

and resistor) with sensor is shown in figure-4.

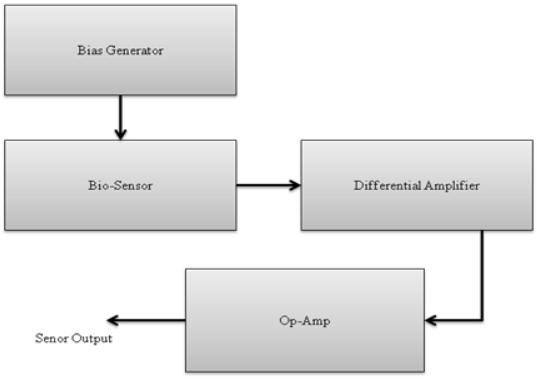


(Fig. 4. Bias circuit)

The output of bias circuit shown in figure-4 is taken from node "*X*". The output is connected with an input of a single ended output differential amplifier. Here differential amplifier is used to detect sensor output and amplify sensor output. The output swing and gain of differential amplifier output is enhanced by adding a suitable gain stage (op-amp). Op-amp used is a traditional two stage single ended differential amplifier [8]. Full circuit of differential amplifier is shown in figure-5. Complete block diagram of the proposed circuit is shown in figure-6.



(Fig. 5. Differential amplifier)



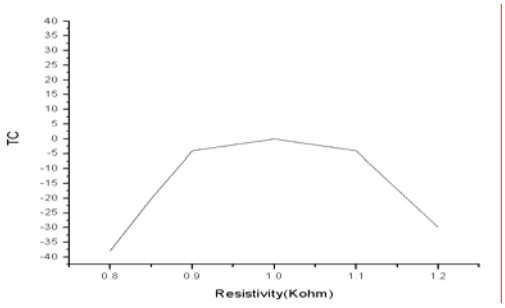
(Fig. 6. Block Diagram of complete circuit)

Parameters	Value
Av	≈ 60 db
PM	≈ 75º
OCMR	≈ 3V
$f_{3\text{-db}}$	≈ 1 KHZ
f_{UGB}	≈ 20 MHZ
ICMR	≈ 1.5 V

(Table-1)

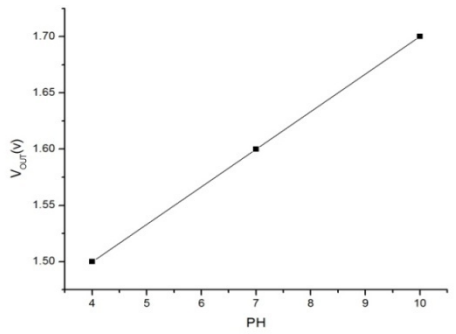
V. Simulation Results-

As mentioned previously, current through the constant current source is controlled by a resistor "*R*". So the magnitude of current must be stabilized with respect to process variation. This can be accomplished by using a process variation independent resistor. Mathematically "*TC*" variation is shown in equation-4. The simulated resistor "*R*", "*TC*" variation with temperature is shown in figure-7.



(Fig. 7. TC variation)

From figure-7, it can be observed that "*TC*" variation is nominal as compared to a simple poly-resistor (1 kohm) "*TC*" variation (typically ≈ 400ppm/^{o}C). The response of the complete circuit with read-out bias circuit is shown in figure-8.



(Fig. 8. Read-out response)

Total circuit is designed using AMS 0.35μm CMOS technology. ISFET is fabricated using 5μm technology of CEERI. Macro-model of ISFET is used for co-simulation with read-out bias circuit. In the macro-model noise and charge associated with the oxide and silicon is not included. Thus noise (typically low frequency) generated by sensor limits the performance of the read-out bias circuit. The differential amplifier used is having a single ended output, thus has poor performance from noise point.

VI. Conclusions-

Macro-model of ISFET sensor has improved the performance prediction of readout bias circuit after design. So the response can be further improved by improvising additional parameters like noise, leakage current etc in the macro-model. Saturation current through ISFET is controlled by process independent series-parallel combination resistor. The area occupied by proposed read-out bias circuit is 0.02 mm^2.

VII. Acknowledgements

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VIII. References-

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