A ±0.6V Low Input Offset, Low Noise Folded Cascode Operational Amplifier for Bio-Medical Applications

First A. Anil K. Saini, Second B. Kapil K. Rajput

IC Design Group

Central Electronics Engineering Research Institute (CEERI), Pilani, 333 031 India , Council of Scientific and Industrial Research (CSIR)

Abstract: **This paper describes a folded cascode operational amplifier (op-amp) for low power, low-offset with ±0.6V supply voltage, designed in a 180nm CMOS process. Design strategy is discussed for reducing input-referred offset and noise. Here optimization for offset and noise has been done using Pelgrom's device mismatch model to avoid trimming and chopper circuitry.**

***Index Terms*—CMOS, mismatches, op-amp, random offset.**

I. Introduction

Modern wireless communication and Bio-medical applications require analog circuit with low power operation. When amplifiers are used in Bio-medical applications, low input offset, low noise and simultaneously low power consumption are essential specifications in area of battery operated systems like pacemakers, blood flow meters, auditory stimulators etc. [1]. The input offset voltage is result of systematic and random offset voltage. Systematic offset voltage arises due to improper design of circuit. While, random offset voltage is an unwanted quantity, which is generated at the time of fabrication in devices mismatch. Random offset voltage occurs due to threshold voltage and dimensions mismatch in input differential pair and current load. A lot of work has been done to improve the performance of analog circuits by minimizing input offset voltage of op-amp. Trimming, auto zero and chopper stabilization are among the popular available techniques for reduction of input offset voltage of op-amp. In literature, to achieve the offset voltage below 1 mV, researcher used trimming and chopper stabilization when in range of 100 μV offset voltage is required. In semiconductor industry, trimming is very popular technique to have an op-amp with less than 1 mV offset voltage. In this technique offset voltage is controlled by resister array with the help of digital controlled circuit. This leads to an extra circuit which increases both the cost and power consumption. Significant work has been done to explore the causes of mismatches on device level, original work done by K.R.Lakshmikumar et al, M.J.M.Pelgrom et al, and later by many authors [2, 3].

Technology scaling limits the signal swing, i.e. noise margin is reduced which introduces the challenge to designer. All the input transistors introduce the equivalent noise, strongly affected by device fabrication and load. Similar to the offset voltage, noise is also random effects and can be modeled by statistically. The noises degrade the performance of the circuits when used in communication, audio application and biomedical applications. Low noise circuits are essential for such kind of applications. Here in this work, we have correlated the noise with input offset voltage and reduced the noise at high frequency.

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F.A. Anil K. Saini is with central electronics engineering research institute, Pilani, India (email: aksaini@ceeri.ernet.in).

S.B. Kapil K. Rajput is with central electronics engineering research institute, Pilani, India (email: kapilrjpt@gmail.com).

II. Transistor Mismatch Parameters

The matched pair of two identical transistors with zero source-bulk bias is modeled by the random variation of threshold voltage differences ΔV_T and current factor differences $\Delta\beta$. These random differences have normal distribution with zero mean and a variance dependent on the device area $W \cdot L$ [4].

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}} \quad (1)$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{W \cdot L}} \quad (2)$$

Where A_{VT} and A_β are the technology dependent constants for threshold voltage and current gain factor.

The approximated standard deviation of the relative drain-source current error and the gate-source voltage error can be described by the following equations [5].

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \frac{1}{\sqrt{W \times L}} \frac{2A_{V_{TH}}}{V_{GS} - V_{TH}} \quad (3)$$

$$\sigma(\Delta V_{GS}) = \frac{A_{V_{TH}}}{\sqrt{W \times L}} \quad (4)$$

The above equations are valid for pair of matched transistors for all regions of operations. Eq. (3) is approximated for equal voltage biased transistors and Eq. (4) for equal current biased transistors, which are illustrated in Figs. 1 and 2, respectively [5].

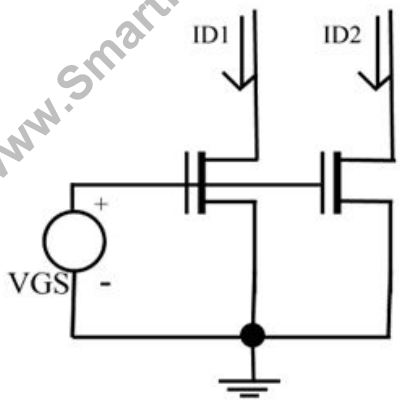

Fig. 1. Transistors biased by the same voltage

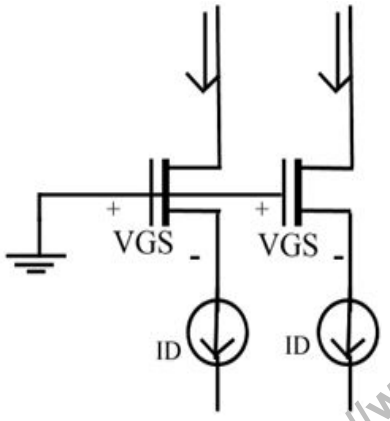

Fig. 2. Transistor biased by the same current

During the design of an analog CMOS circuit, the designer has the freedom to choose the current, width (W) and length (L) of each transistor. For a given current and bias point (V_{GS} - V_{TH}), only the aspect ratio (W/L) of the device is fixed, but the width or the length can still be chosen freely. It can be seen from Eq. 3 and 4 mismatches in drain-source current and threshold voltage are inversely proportional to device area.

III. Circuit Overview

Fig.3 shows the proposed folded cascode op amp. In this architecture, three cascode transistors in output stage helps to reduce total overdrive voltage range. In Fig. 3 M4-M5 and M6-M7 transistors construct p-type wide-swing cascode current mirror. The voltage drop across M4, M6 and M8 are (V_t+ΔV) and ΔV. The proposed folded cascode op amp shown in Fig. 3 has following reasons to full-fill the requirement:

1) The NMOS input pair has lesser input offset than PMOS input pair.
2) The output stage with high swing current mirror and three stage cascode consumes proper overdrive voltage with ±0.6V supply.
3) The NMOS flicker noise coefficient KFn is smaller than that of PMOS, which is helpful for achieving lower flicker noise.
4) NMOS has a higher transition frequency f_T than PMOS, which can help to maintain high bandwidth.

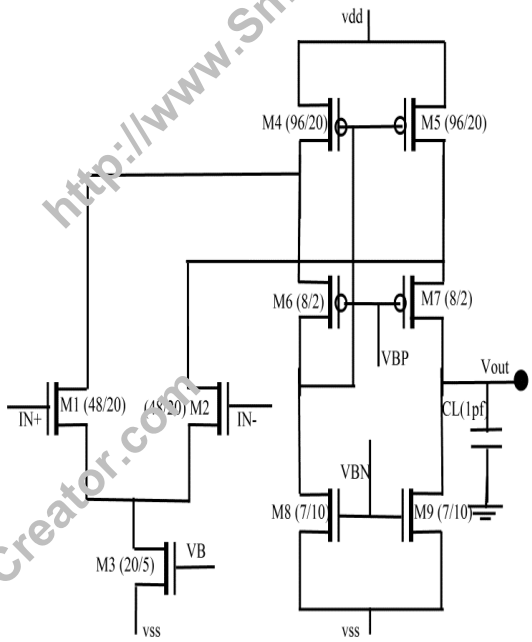

Fig. 3 Proposed folded cascade op amp

The input-referred random offset of the circuit in Fig. 3 can be described by [6]:

$$V_{OS} \approx \Delta V_{t1,2} + \Delta V_{t4,5}\frac{g_{m4}}{g_{m2}} + \Delta V_{t8,9}\frac{g_{m8}}{g_{m2}} + \frac{V_{ov1,2}}{2} \times \left[\left(\frac{\Delta\left(\frac{W}{L}\right)_{1,2}}{\left(\frac{W}{L}\right)_{1,2}} + \frac{\Delta\left(\frac{W}{L}\right)_{4,5}}{\left(\frac{W}{L}\right)_{4,5}} + \frac{\Delta\left(\frac{W}{L}\right)_{8,9}}{\left(\frac{W}{L}\right)_{8,9}}\right)\right] \quad (5)$$

The expressions for thermal and flicker noise of a MOS are described as [7]:

$$\overline{V_{thermal}^2} = 4kT\left(\frac{2}{3}g_m\right)r_O^2 \quad (6)$$

$$\overline{V_{flicker}^2} = \frac{KFn}{C_{OX}WL}\cdot\frac{1}{f} \quad (7)$$

IV. Design and Simulation Results

We designed above proposed low supply voltage folded

cascode op amp based on 180nm Twin well CMOS process. It can be observed from Eq. 5, 6 and 7 that input offset voltage, thermal and flicker noises depend upon device aspect ratio and device area respectively. Using Pelgrom's device mismatch model, the input offset voltage can be optimized for proposed op amp.

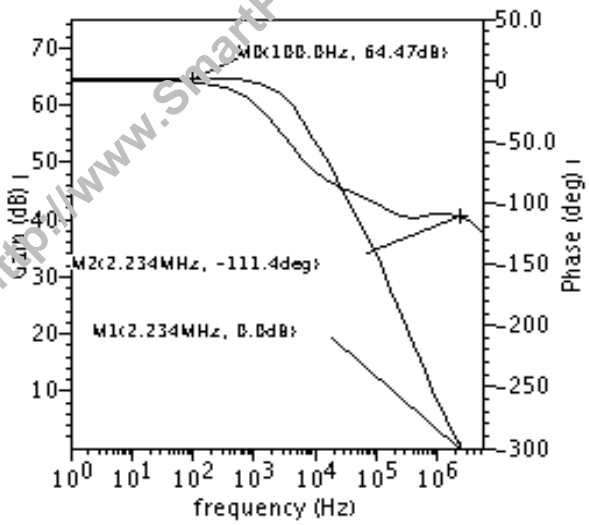

Fig. 4 Simulation results of AC performance

The efforts taken in this design to reduce random input offset voltage are also helpful in minimizing the noise. Fig. 4 shows gain and phase simulation results, the designed amplifier was targeted to the phase margin ≥ 60° at ±0.6V power supply.

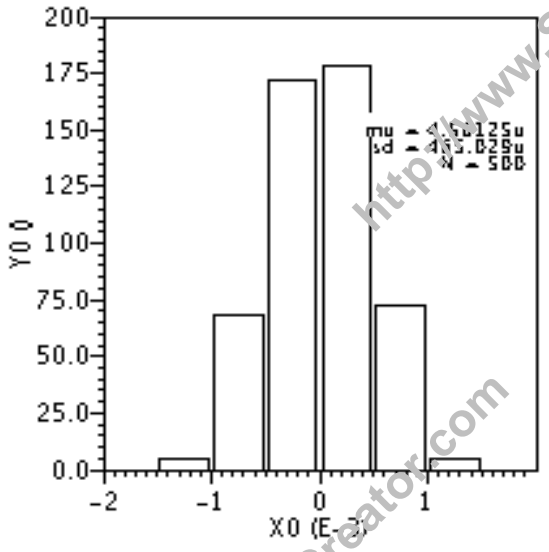

Fig. 5 Input offset voltage

The input offset voltage has been optimized upto 465µV, Monte Carlo simulation (for 500 run) and input common mode range (ICMR) simulation results are shown in Fig. 5 and 6 respectively. The equivalent referred input noise simulation is plotted in Fig. 7. The simulated results are summarized in Table 1 and a comparison is made with reported architecture in different technology for different supply.

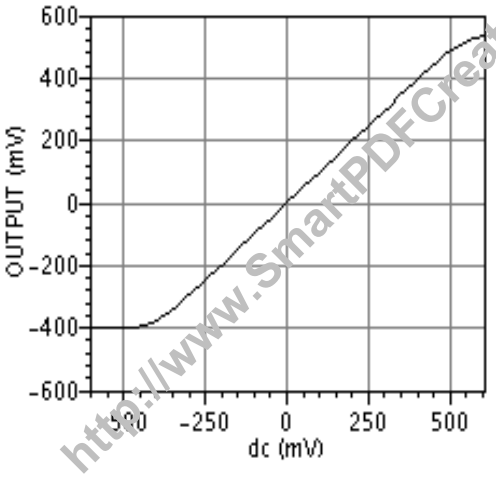

Fig. 6 Input common mode range

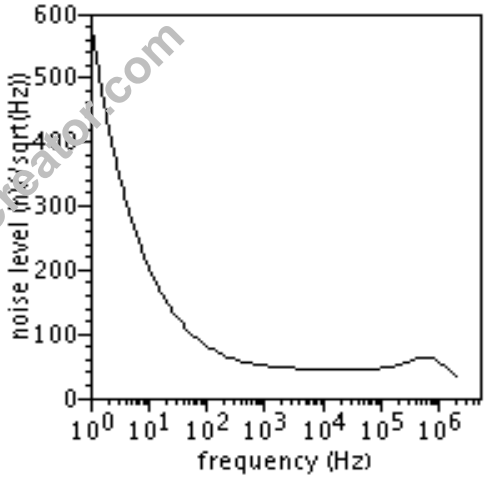

Fig. 7 Equivalent input referred noise

Table 1 Summary of simulated results and comparison with low voltage op-amps

Technology	0.35µm[6]	90nm[8]	180nm
Supply Voltage (V)	3.3	0.5	±0.6
Load cap. (pf)	-	3	1
DC gain (db)	100	41.7	64.5
Unity gain Frequency(MHz)	300	56	2.234
Phase margin (°)	-169.4	-	68.77
ICMR (V)	-	-	-0.38 to 0.46
Offset (mV)	10	-	0.465
Input refered noise(nV/sqrt(Hz))	2	-	3.2
Power Consumption (µW)	-	70	6

V. Conclusion

A low offset low noise folded cascode op amp is designed in 180nm CMOS Twin well process. Pelgrom's device

mismatch model is used in design of op amp to minimize input offset voltage as well as total input referred noise. The required minimum supply voltage is reduced to ±0.6V by exploiting the wide-swing cascade current mirror. The proposed op amp is good choice for Bio-medical application with low input offset, low input referred noise and 6µW power.

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REFERENCES

[1] Sandro A.P. Haddad and Wouter A. Serdijn, *Ultra Low-Power Biomedical Signal Processing: an analog wavelet filter approach for pacemakers,* Springer, 2009.

[2] K.R. Lakshmikumar, R.A. Hadaway, M.A. Copeland, "Characterisation and modeling of mismatch in MOS transistor for precision analog design," IEEE *J*. Solid-State Circuits, vol. 21, no. 6, pp.1057-1066, Dec 1986.

[3] M.J.M. Pelgrom,, A.C.J. Duinmaijer, A.P.G. Welbers, "Matching properties of MOS transistors," IEEE *J*. Solid-State Circuits, vol. 25, no. 5, pp. 1433-1439, Oct 1989.

[4] P. Kinget, M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits," IEEE 1996 Custom Integrated Circuits Conference, pp. 333-336.

[5] J.P. Martinez Brito, S Bampi, "A DC offset and CMRR analysis in a CMOS 0.35µm operational transconductance amplifier using Pelgrom's area/accuracy tradeoff," Microelectrons. J., vol.40, issue 9, pp. 1281-1292, Sept. 2009.

[6] Zhu Z, Tumati R, Collins S, Smith R, Kotecki D.E., "A low-noise, low-offset operational amplifier in 0.35 µm technology,", 13th IEEE Int. Conf. on Electronics, Circuits, and Systems (ICECS); Nice, France. Dec. 10–13, 2006.

[7] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Inc., 2000.

[8] G.A.V. Sai Praneeth, Anil K. Saini, "A Self Biased Operational Amplifier at Ultra Low Power Supply," The 16th IEEE Int. Conference on Electronics, Circuits and Systems, Dec 2009, Hammamet, Tunisia (selected for presentation).

Anil K. Saini was born in Uttar Pradesh India, on June 15, 1978. He received the M.Sc and M.Tech degree in Physics and Solid State Electronics Materials from Indian Institute Of Technology Roorkee, India, in 2000 and 2003 respectively.

In the fall of 2004 he joined Cadence Design System, where he worked in Logic Design Verification. In 2005, he joined the Integrated Circuit Design Group at Central Electronic Engineering Research Institute a CSIR laboratory as SCIENTIST. His work is focused on Mixed-Signal circuit design for sensor interface. Another field of research is low voltage low power analog circuit for Bio-medical applications.

Kapil K. Rajput has completed his Master of Science in Electronics from C.C.S. University Meerut in 2005 and Master of Technology in Microelectronics from Jaypee Institute of Information Technology University Noida in 2008 respectively. Since then he has been working as research assistant for design and development of analog mixed signal circuits with IC Design Group, Central Electronics Engineering Research Institute Pilani (Rajasthan). His main research interests are analog mixed signal circuit design and high performance semiconductor devices.