Electrical characterization of thin thermally grown SiO_2 on epitaxial 4H-SiC (0001) substrate with varying oxide thickness

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Abstract:

Electrical conduction across thermally grown silicon dioxide on Si-rich 4H-SiC (0001) surface has been experimentally analyzed on the basis of measured I-V characteristics for varying oxide thickness from 23 nm to 61.4 nm. Validity of current conduction mechanisms involving Fowler-Nordheim (F-N) tunneling, Schottky emission (S-E) and Poole-Frenkel (P-F) conduction has been established quantitatively on the basis of electric field and the oxide thickness employing forward I-V characteristics. F-N tunneling has been found valid for all fields in case of oxide thickness below 30 nm. For thicker oxides (up to 56.6 nm) F-N tunneling occurs in presence of high electric fields only, exposed a bulk limited conduction mechanism. An electrode limited conduction mechanism has been observed in case of Schottky emission and Poole-Frenkel conduction. At lower fields Schottky emission dominates because effective conductivity depends strongly on the barrier between the metal and insulator and has the proclivity to occur for insulators with fewer defects while Poole-Frenkel conduction takes place at higher electric fields due to field-enhanced excitation of trapped charge in to the conduction band of SiO_2 indicate the presence of electron traps in bulk of thermally grown SiO_2.

Keywords: 4H-SiC; wet oxidation; MOSiC structure; conduction mechanism

1. Introduction:

Novel materials are continually researched in electronics, especially in such area of applications where silicon properties have never been satisfactory. It has been known that SiC is of great interest for high-power, high-temperature, and high-radiation electronics [1]. 4H-SiC is one of the polytypes of SiC which has a large bandgap, the highest electron mobility among hexagonal polytypes of SiC, a high value of critical

electric field, high saturation velocity of electrons and high thermal conductivity [2]. Among the group of wide band gap semiconductors, SiC competes owing to its unique capability of oxidation in the form of SiO_2 making it an obvious choice for the replacement of mighty silicon MOS devices. To fabricate these devices, a high quality gate oxide is much required. It serves as an insulating layer in order for the gate to support a high transverse electric field so that the channel conductance can be modulated [3]. If the oxide quality is poor, current will be leaked through the oxide. This leakage current could have a disadvantageous effect on the device performance during operations. The oxidation growth mechanism as well as MOSiC characterization on SiC surfaces however has been at its developmental stage. The gate current might affect the performance of devices that employ metal oxide silicon carbide (MOSiC) structure, and it can be dominating factor in device down-scaling. The feasibility with MOS devices that fabricated with thin oxides was demonstrated 10 years ago [4]. Presently, thermal grown SiO_2 with an ultra-low leakage current is commonly used as the material for the gate oxide for device application [5-10].

The present work is an experimental addition to the prevailing knowledge of current conduction mechanism as the function of thermally grown SiO_2 thickness. The gate current might affect the performance of devices that employ Metal Oxide Semiconductor (MOS) structure, and it can be dominating factor in device down-scaling [4]. Therefore a precise knowledge of the current conduction through the potential energy barrier for different oxide thickness has become impartment to understand oxidation behavior of SiC. The basic principle of reducing the MOS scaling indicate that when we reduce the lateral dimension of MOS devices, the vertical dimension must be modified according to the device dimension. This reduction in oxide thickness causes a different type of current conduction through this insulator, which depends exponentially on the thickness of the oxide. The inter band tunneling occurs because of the finiteness of the height and width of the oxide barrier. It can be either direct tunneling (DT) [11], Fowler-Nordheim (FN) tunneling [12, 13] Schottky emission (SE) [14, 15] or Poole-Frankel (PF) conduction [16-17] depending upon the magnitude of oxide thickness, defect at interface and polarity of the applied gate voltage. The present work deals with experimental justification to crop up the above conduction model within the oxide thickness limit.

In this paper, we report systematic investigation of current conduction mechanism produced by Fowler-Nordheim tunneling, Schottky emission and Poole-

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Frenkel conduction across MOSiC structure with varying oxide thickness on device grade epitaxial 4H-SiC substrate. Wet thermal oxidation technique has been used to grow SiO_2 at fixed temperature of 1110^0C for different oxidation time. Experimental details of sample preparation, fabrication of MOSiC structures and I-V measurement methodology are given in the next section. Current conduction models, acquired results with discussion are mentioned in the section thereafter which is followed by conclusion.

2. Experimental details

2.1 Fabrication of MOSiC structure:

A 2″ diameter 4H-SiC 50 μm epitaxy wafer of n/n^+ type 8^0 off-axes oriented were purchased from CREE Research Inc. USA. The wafer has been cut into several pieces using special dicing blade from M/s DISCO Japan [1]. Prior to loading in a quartz furnace for the oxidation, RCA chemical cleaning treatment was given to all the samples. Samples were loaded for oxidation at 800^0C with a flow of nitrogen. Wet thermal oxidation has been performed at 1110 ^{0}C and samples were unloaded at 800^0C in nitrogen flow. This was repeated for each batch of samples with varying oxidation time from 30 minutes to 360 minutes. A thoroughly optimized oxidation process is described in details elsewhere [18]. Oxide thickness on each sample was recorded using Ellipsometer. Figure 1 shows the variation of oxide thickness as a function of oxidation time on Si-face and C-face.

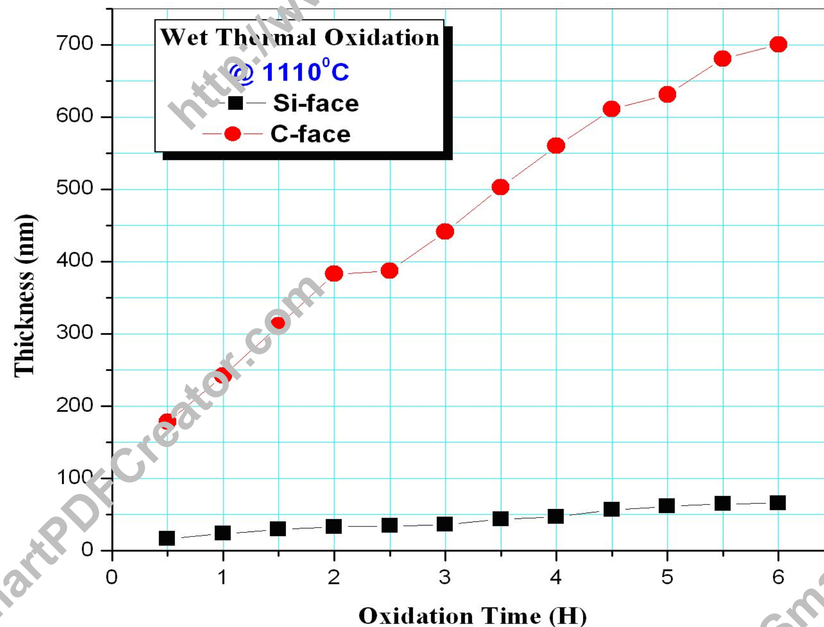

Figure 1 Oxidation thickness with oxidation time

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In order to fabricate the MOSiC structure oxide layer from the c-face or n^+ side of 4H-SiC has been removed using buffer oxide etchant (BOE) by protecting the si-face with photoresist. Ohmic contact has been performed on the c-face with composite layer of Ti (300Å) and Au (2000 Å) by e-Beam evaporation method in the vacuum range of 10^{-7} torr. Gate metal contact over the different thickness of SiO_2 has been performed using Ni (1500 Å) by the same metallization method with same vacuum range. Figure 2 shows the schematic of MOSiC structure. Chips carrying arrays of MOSiC structures on individual chip have been packaged on TO-8 headers. Packaged devices has been tested and characterized by fully automated HP 4140B pA meter/ DC voltage source on LabVIEW platform.

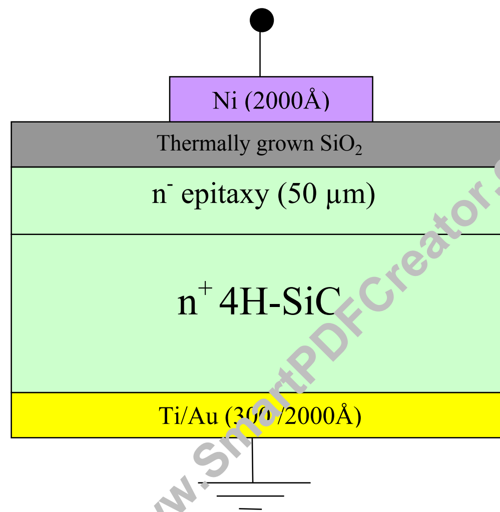

Figure 2. Schematic of metal-oxide-silicon carbide (MOSiC) structure

3. Results and discussion:

3.1 Measurements of forward I-V characteristics

The life time of particular gate oxide thickness is determined by the total amount of charge carriers that flow through the gate oxide under the influence of electric field. Ideally, an oxide layer does not allow charge carrier to pass through. There are several current conduction mechanisms which allow charge to pass through oxide. It has been previously reported that for the oxide thickness greater than 5 nm [13] up to 50 nm [19] current conduction is explained by Fowler- Nordheim tunneling and in the same sequence for the oxide thickness greater 50 nm is explained by Schottky emission [19]. If the oxide thickness is greater than 50 nm having some trapped charge inside it, can be governed by Poole-Frenkel conduction model. On the other hand, current conduction for the ultra thin oxide layers less than 5 nm, has been termed as direct

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tunneling [20].Fig. 3 shows the current voltage characteristics across MOSiC structure for the different gate oxide thickness starting from 23.7 nm to 61.4 nm. This plot revealed that resistance of the bulk material increase with oxide thickness provides the knowledge of current conduction mechanism through insulator.

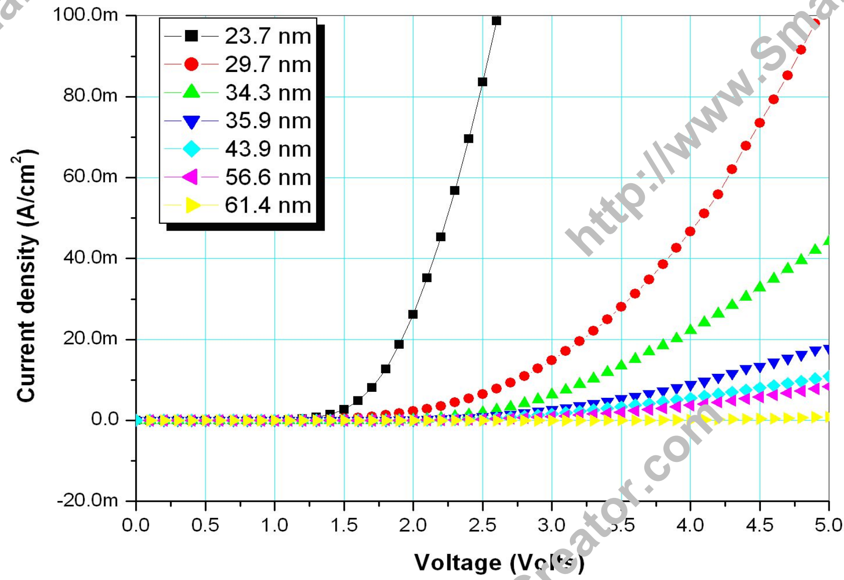

Figure 3 Current-Voltage characteristics across MOSiC structure over different oxide thickness.

3.2 Theoretical models of current conduction

According to the current conduction model, the plot of ln (J/E^2) versus $1/E$ (called F-N plot), ln (J) versus $E^{1/2}$ (called Schottky emission plot), and ln (J/E) versus $E^{1/2}$ (called Poole-Frenkel conduction plot) should be linear. This linearization of existing plot over the oxide thickness has been taken in to account. The linear relationship between current and voltage can not be observed directly in experimental results. This experimental observation explained that there is no significance of direct tunneling for oxide thickness greater than 23.7 nm.

(a) Fowler-Nordheim tunneling:

In the F-N tunneling oxide potential barrier is usually assumed to be a triangular one, free of charge gate insulator. As a consequence, when we apply a uniform electric field across the MOSiC structure, thickness of the potential barrier and the potential $\phi(x)$, at the distance x from silicon carbide/oxide interface vary linearly with the applied voltage.

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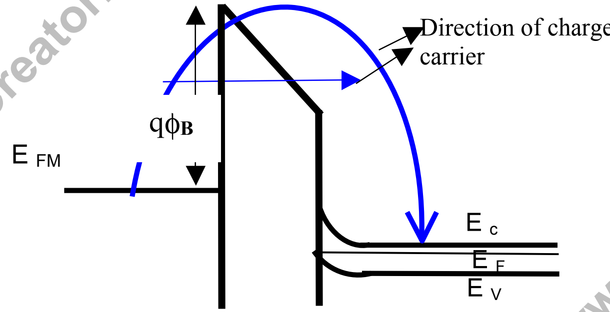

Figure 4 Triangular shape of energy band diagram for F-N tunneling.

The insulating region is separated by an energy barrier with barrier height $q\phi_B$, measured from the Fermi energy of metal to the conduction band edge of the insulating layer. Electrons tunnel from metal to semiconductor. The current density (J) can be calculated as the function of applied voltage to consider some assumptions like Effective-mass approximation, parabolic bands and Conservation of parallel momentum [21]. The net tunneling current density from metal to semiconductor can be written as the net difference between current flowing from metal region to semiconductor region and vice versa. This expression for current density is usually written as an integral over the product of two independent parts which only depend on the energy perpendicular to the interface i.e. the transmission coefficient T (*E*) and the supply function N (*E*).

$$J = \frac{4\pi m_{\text{eff}}\, q}{h^3} \int_{E_{\min}}^{E_{\max}} T(E)\, N(E)\, dE \tag{1}$$

This expression known as TSU-ESAKI formula [21]. The calculation of current density requires not only the knowledge of the energy dependent transfer coefficient**,** but also the energy dependent electron probability (supply function), Using the Tsu-Esaki formula for current density the Fowler-Nordheim formula can be derived as:

$$J(E_{\text{diel}}) = A E_{\text{diel}}^{2} \exp\left(-\frac{B}{E_{\text{diel}}}\right) \tag{2}$$

Where, E_{diel} electric field in oxide**,** A and B are constants dependent on barrier configuration for oxide layer separated by metal and semiconductor. The constants *A* and *B* are

$$A = \frac{q^3 m_{\text{eff}}}{8\pi m_{\text{diel}} h q \Phi_B} \qquad B = \frac{4\sqrt{2 m_{\text{diel}} (q\Phi_B)^3}}{3\hbar q} \tag{3}$$

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Where ϕ_B is the height of the potential barrier measured from the Fermi level of metal to the conduction band in the dielectric m_{iff} effective electron mass in electrode material m_{diel} effective electron mass in the dielectric material.

(b) Schottky emission:

Image charges build up in the metal electrode as well as at oxide silicon carbide interface as carriers approach from metal through insulator to conduction band of silicon carbide. The potential associated with these charges reduces the effective barrier height by the amount of $\Delta\phi_B$. This barrier reduction tends to be rather small compared to the barrier height itself. Fig 5 (a) shows the energy band diagram accomplished with image charge where as fig 5 (b) shows most feasible direction of charge flow due to barrier height lowering.

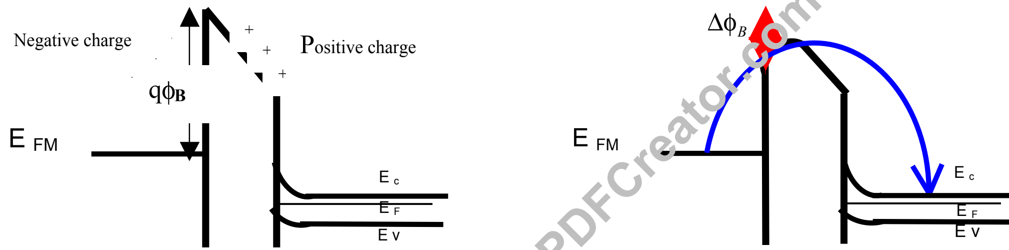

Figure 5 (a) Energy band diagram for Schottky emission **Figure 5 (b) direction of charge flow due to barrier lowering**

The mode of electric conduction through the insulator is revealed by linearizing the current density versus electric field curve in accordance with the Schottky emission equation [22] described as

$$J = A^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_i}}{kT}\right] \tag{4}$$

Where J is the current density; A^*, the Richardson constant; T, the absolute temperature; q, the electronic charge; ϕ_B, the potential barrier at metal/oxide interface; E, the applied electric field; ε_I, is dielectric constant and k, the Boltzmann constant.

(c) Poole-Frenkel Conduction:

The Poole-Frenkel (P-F) conduction mechanism is expected to be dominant in insulating thin films when they have a large trap density and are thick enough to avoid quantum-mechanical tunneling [23]. The high density of traps protect the transport of electrons in the conduction band by drift and diffusion mechanisms and trapping and

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de trapping of electrons become the dominant processes that control the conduction-electron density in the insulating films.

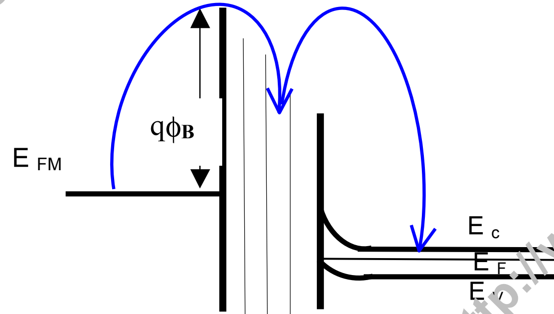

Figure 6 Energy band diagram for trapped assisted Poole-Frenkel conduction.

Trapped assisted tunneling or Poole-Frenkel conduction for thick oxide can be described as [22]:

$$J = E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i}}{kT}\right] \tag{5}$$

Where J is the current density; A^*, the Richardson constant; T, the absolute temperature; q, the electronic charge; ϕ_B, the potential barrier at metal/oxide interface; E, the applied electric field; ε_I, is dielectric constant and k, the Boltzmann constant.

3.3 Conduction mechanisms and experimental results

The interpretation of current conduction mechanisms from the experimental data has been done by using the measured forward I-V characteristics across MOSiC structure. For thin oxide the current flow through the triangular shape of the barrier, is caused by partial conduction according to figure 4. Figure 7 shows that the plot of ln (J/E^2) versus 1/E is linear over entire electric field provide the evidence of F-N tunneling for thin oxide (23.7 nm and 29.7 nm) only. The probability of current conduction through below the conduction band of oxide will be diminishing in case of thick oxide. To conduct the current in case of thick oxide, produced by F-N tunneling mechanism, a high electric field will be required. In high electric field the conduction band of oxide towards the silicon carbide as well as triangular shape of energy barrier will be reduce. As the consequence of this mechanism the plot of ln (J/E^2) versus 1/E is linear over high electric field for thick oxide which is valid up to 56.6 nm as shown in figure 8. There is no F-N tendency has been observed in case of 61.4 nm oxide thickness.

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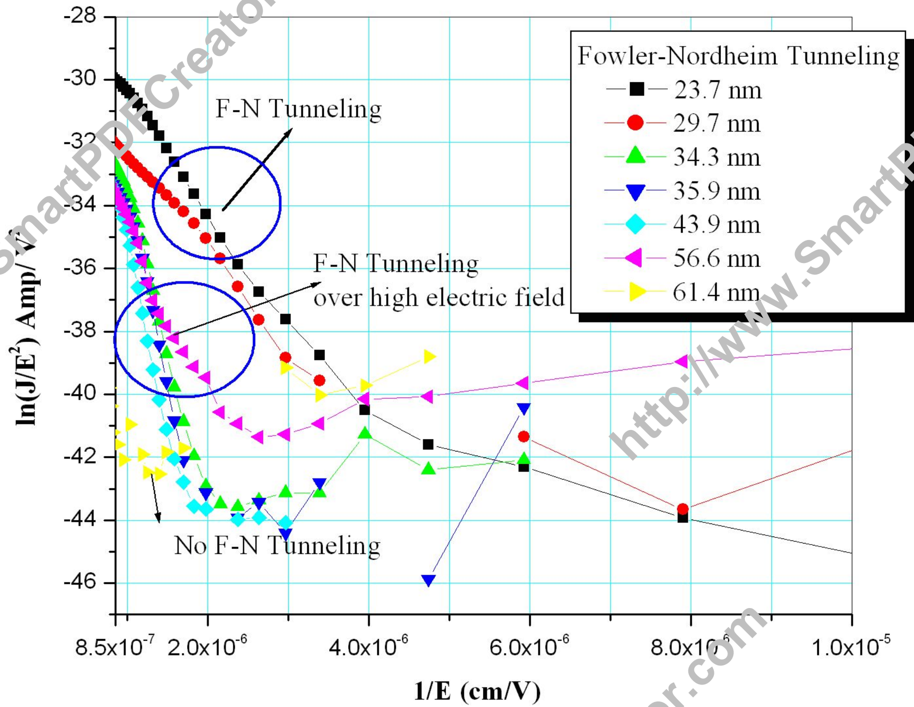

Figure 7 F-N tunneling plot for entire electric tunneling plot over different oxide thickness

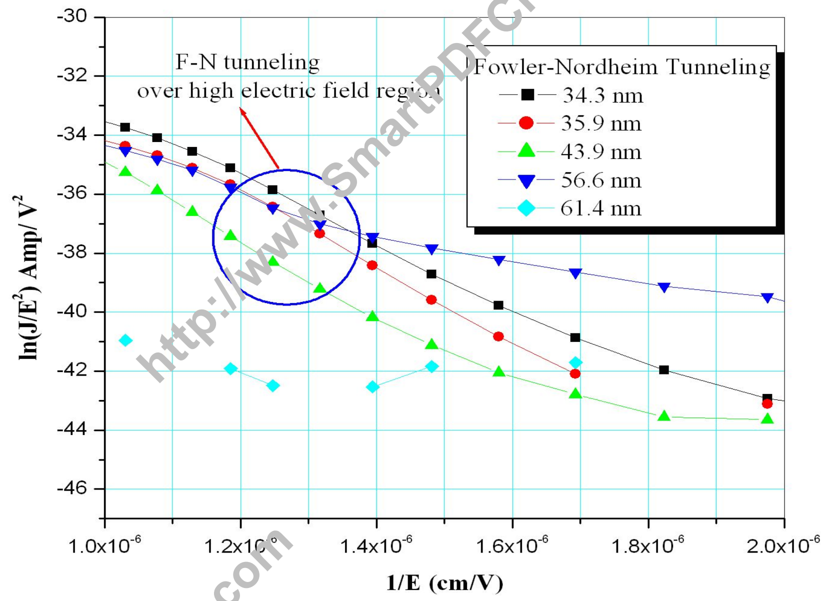

Figure 8 F-N plots in high electric fields region

The Schottky emission is a electrode limited process occurring across the interface between a semiconductor (or metal) and an insulating film as a result of barrier lowering due to the applied electric field and the image force as shown in figure 5 (a) and (b). Since, the S-E current conduction process is an electrode-limited, the conductivity that depends strongly on the barrier between the metal and insulator and

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has the proclivity to occur for insulators with fewer defects. Schottky-emission for all samples has been illustrated in terms of ln (J) versus $E^{1/2}$ plot from the experimental forward current-voltage data which is shown in figure 9. The straight line characteristic at relatively low electric field has been observed experimentally. If the measured value of ln (J) versus $E^{1/2}$ is linear, the conduction mechanism is considered to be a S-E (electrode limited) process. The potential barrier lowering in the MOSiC structures caused by image forces as shown in figure 5 (b) is often neglected in the calculation of the tunneling current, based on an argument that for large barriers in the case of semiconductor and insulator the image-force lowering of the barrier is very small, and this was supported by experimental evidence at the time [4]. In case of very thin oxides, however, this might not be the case, and the barrier lowering can have an impact on the calculation of the tunneling current. Figure 9 shows the S-E characteristics for electric field range 3.036×10^5 V/cm to 4.199×10^5 V/cm for oxide thickness 23.7 nm. Similarly, for rest of the oxide thickness S-E range have been extracted and presented in tab. 1.These observations can be correlated with the conductivity of the SiO_2. Increment in the oxide thickness resulted into wider potential barrier between metal and silicon carbide. Since applied electric field, reduce the barrier height with respect to applied electric field across MOSiC structure (as summarized in table 1) but increment in the effective potential width become dominating factor and finally S-E range vary with oxide thickness

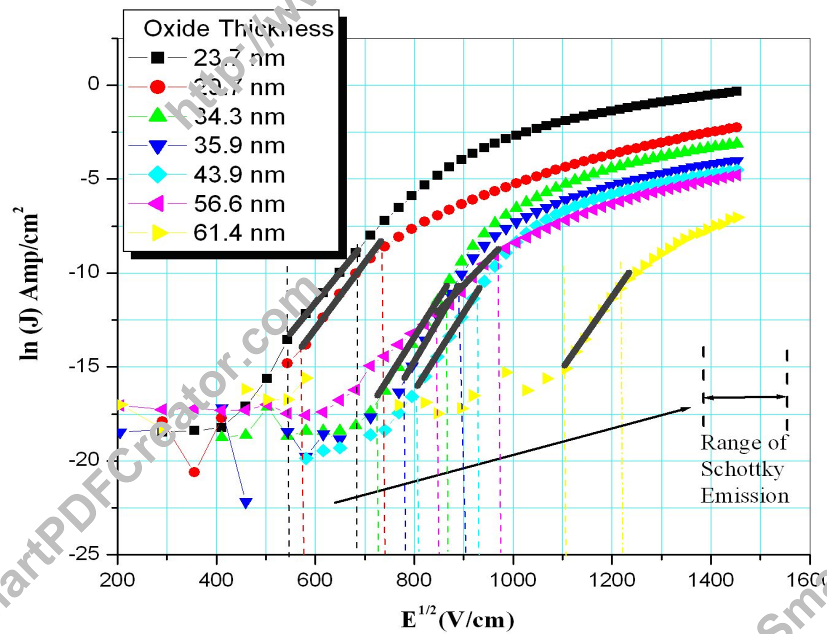

Figure 9 Schottky emission plot for varying electric fields

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Poole-Frenkel conduction results from field-enhanced excitation of trapped charge in to the conduction band of SiO_2 indicate the presence of electron traps in bulk of insulating layer. At room temperature traps do not donate electrons i.e. free electron to the conduction band of silicon carbide or accept electron from valence band i.e. free holes because they are located many k_BT below the conduction band (for donors) and above the valence band (for acceptors). The functional dependence of conductivity upon electric field strength in the different thickness of SiO_2 in MOSiC structure can be differentiate from their different rate of change of conductivity with electric field strength by a plot of ln(J/E) versus $E^{1/2}$, a straight line as shown in figure 10. At field greater than 9.910×10^5 V/cm for oxide thickness 23.7 nm, electrons in the SiO_2 bulk traps gain sufficient energy to be excited to the conduction band of silicon carbide and Poole-Frenkel conduction becomes the dominating conduction mechanism beyond that electric field. Similarly the applied electric field greater than 1.128×10^6 V/cm for 29.7 nm oxide thickness, 1.232×10^6 V/cm for 34.3 nm oxide thickness, 1.301×10^6 V/cm for 35.9 nm oxide thickness, 1.385×10^6 V/Cm for 43.9 nm oxide thickness, 1.458×10^6 for 56.6 nm oxide thickness and 1.755×10^6 V/cm for 61.4 nm oxide thickness shows a typical linear plot of dominating Poole-Frenkel conduction mechanism in thermally grown SiO_2 on thick epitaxial 4H-SiC substrate.

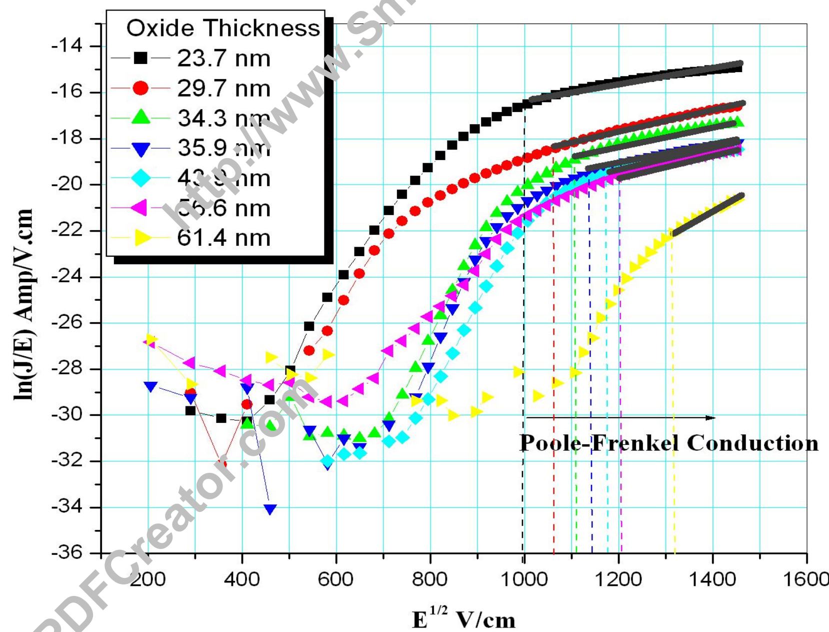

Figure 10 Poole-Frenkel conduction plots for all oxide thickness in MOSiC structure.

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Oxide Thickness (nm)	Schottky emission range (V/cm)	Poole-Frenkel range (V/cm)
23.7	3.036×10^5-4.199×10^5	$> 9.910\times10^5$
29.7	3.352×10^5-5.533×10^5	$> 1.128\times10^6$
34.3	5.340×10^5-7.598×10^5	$> 1.232\times10^6$
35.9	6.129×10^5-8.201×10^5	$> 1.301\times10^6$
43.9	6.546×10^5-8.678×10^5	$> 1.385\times10^6$
56.6	7.281×10^5-9.574×10^5	$> 1.458\times10^6$
61.4	1.223×10^6-1.273×10^6	$> 1.755\times10^6$

Table1. Electric field range for effective conduction mechanism extracted from measured plots.

4. Conclusions:

In this work, current conduction mechanisms have been experimentally characterized on the basis of bulk limited and electrode limited phenomenon across the MOSiC structure with varying oxide thickness. It has been observed that Fowler-Nordheim tunneling is valid up to 30 nm of oxide thickness for entire electric field range while up to 56.6 nm in high field region. In case of thick oxide (61.4 nm), F-N plot terminate to its limitation, revealed a bulk limited behavior. Electrode limited tendency has been observed in both Schottky emission and Poole-Frenkel conduction. Schottky emission can be seen to be dominating mechanism in low fields while Poole-Frenkel conduction dominates in high fields for thickness of thermally grown SiO_2.

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